

# AM64x/AM243x EVM BOARD

## PROC101C

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REV	C
VER	1.1

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Size	Variant Name = PROC101C(004) TMD564EVM	Rev
C		E2
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## REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	11th MARCH 2022	Drafted from "PROC101B_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	11th MARCH 2022	Removed Voltage Monitor circuit & added RC Delay Circuit for power down sequence requirement Fixed Power down sequence issue seen on AM243x REV B	Mistral Design Team	AJIT MB	AJIT MB
0.3	11th MARCH 2022	Updated schematics to support PG2 Silicon	Mistral Design Team	AJIT MB	AJIT MB
1.0	30th MARCH 2022	Baselined and Released	Mistral Design Team	AJIT MB	AJIT MB
1.1	5th AUG 2022	Updated SoC Part Number and OPN Details Updated SoC Symbol for Reserved pins	Mistral Design Team	AJIT MB	AJIT MB

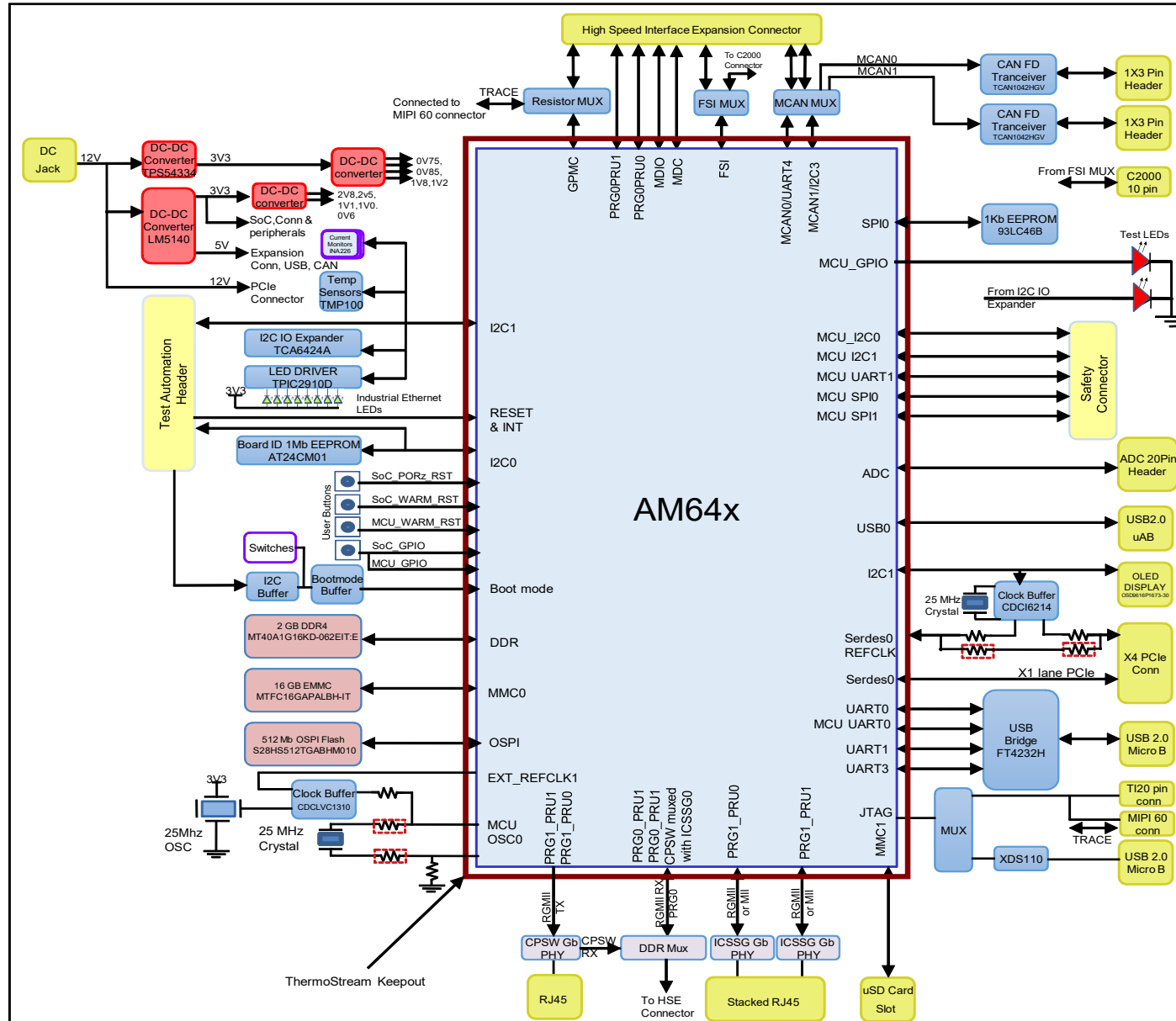
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Title REVISION HISTORY

Size	Variant Name = PROC101C(004) TMD564EVM	Rev
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## BLOCK DIAGRAM\_AM64x\_EVM



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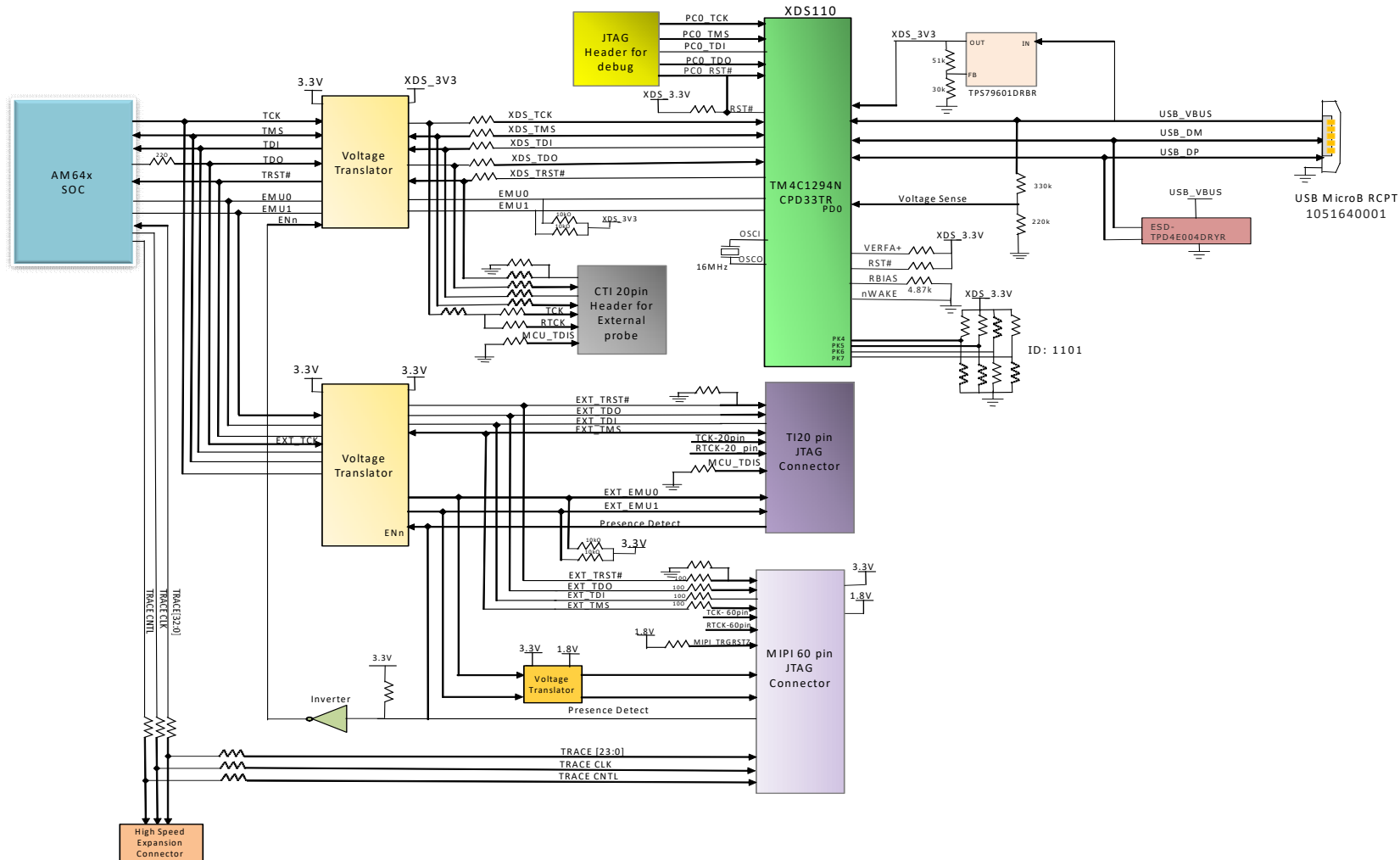
Title	BLOCK DIAGRAM_CP BOARD
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Size	
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C	Variant Name = PROC101C(004) TMD564EVM	E
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Date:	Thursday, August 18, 2022	Sheet	3	of	40
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# BLOCK DIAGRAM\_XDS110



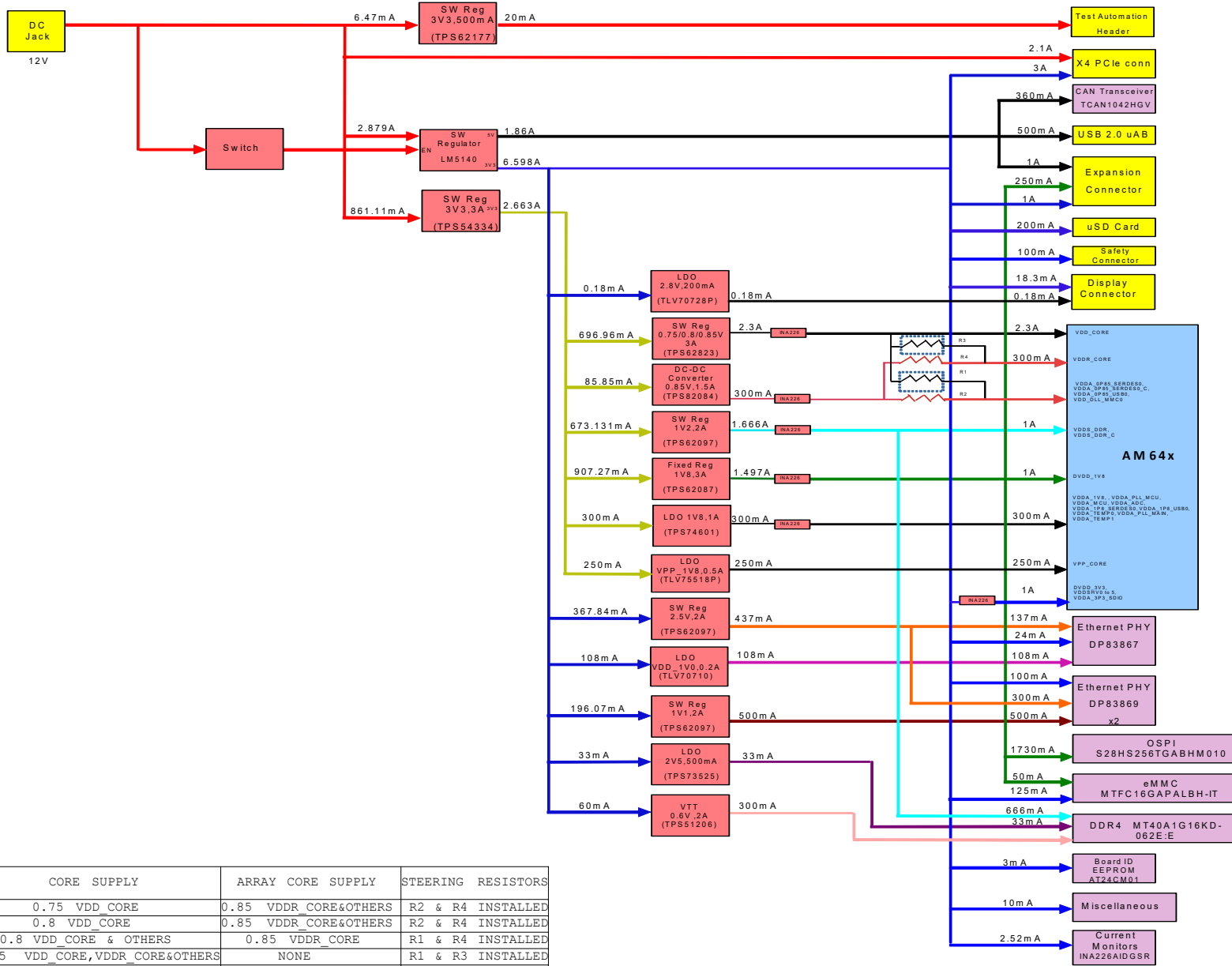
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Title BLOCK DIAGRAM\_XDS110

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# POWER FLOW DIAGRAM



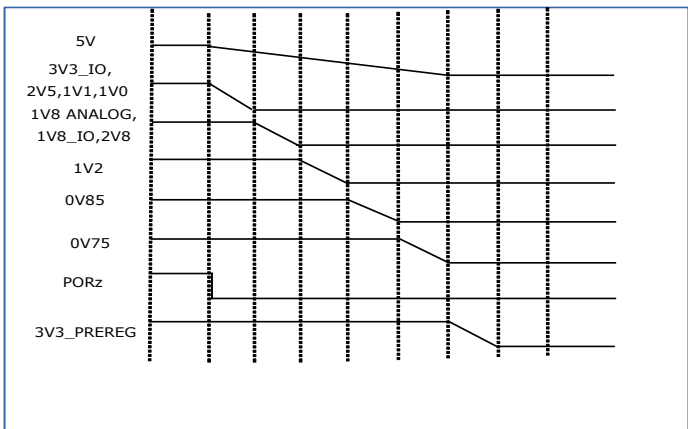
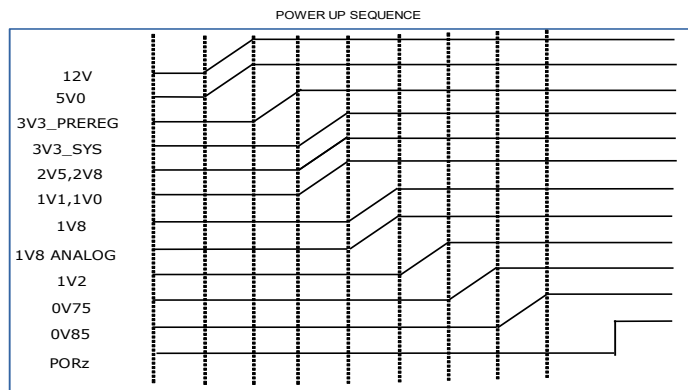
CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE, VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

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Title POWER FLOW DIAGRAM

Size	Variant Name = PROC101C(004) TMD564EVM	Rev
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[illegible]

## GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI0_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via OE res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCl_e_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN transceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN transceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESETh	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Selection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

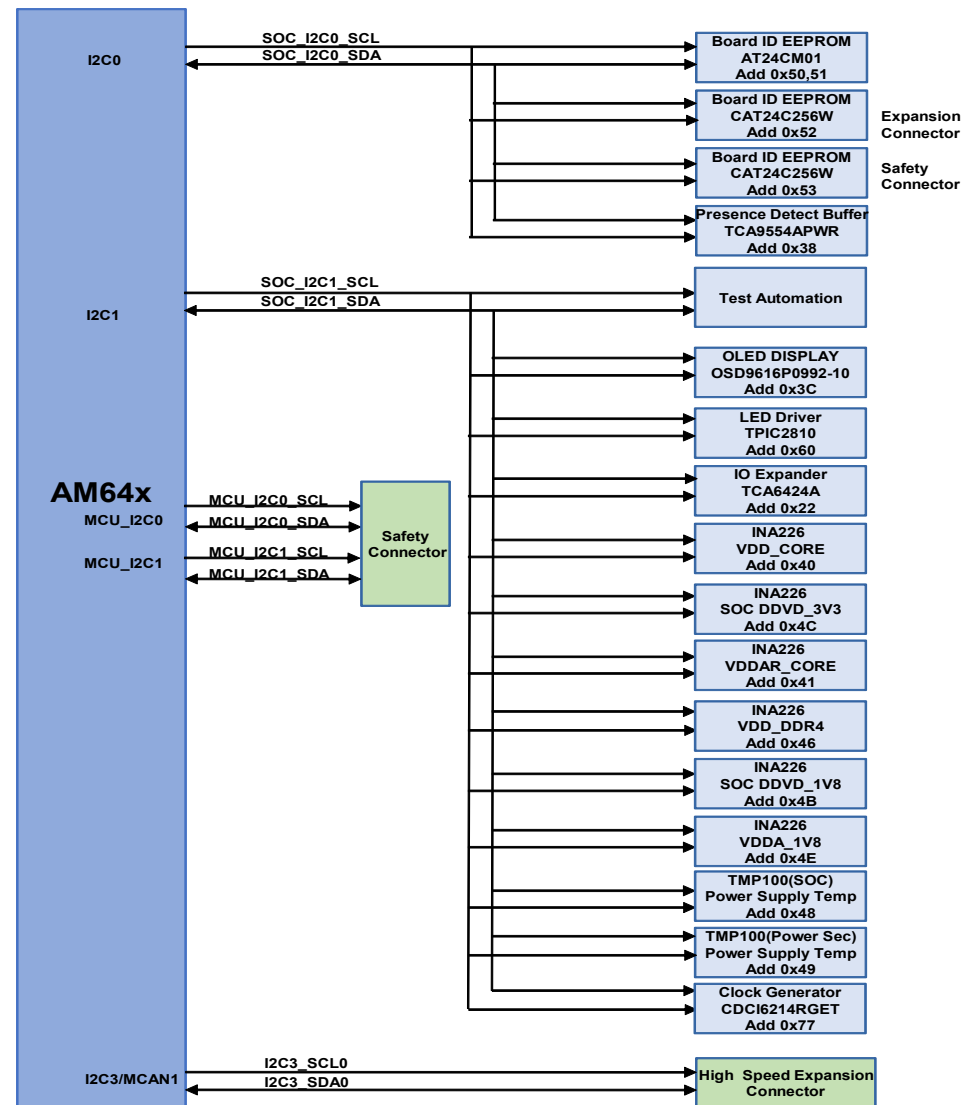
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Title GPIO MAPPING TABLE

Size	Variant Name = PROC101C(004) TMD564EVM	Rev
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# I2C TREE



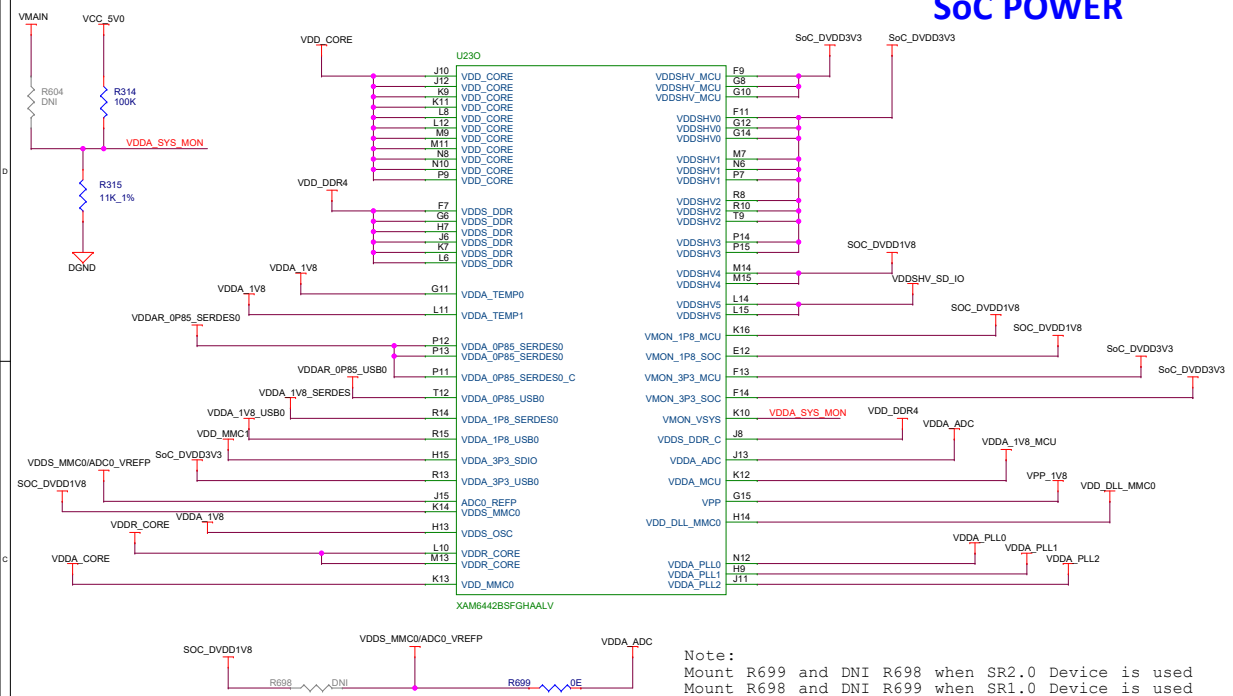
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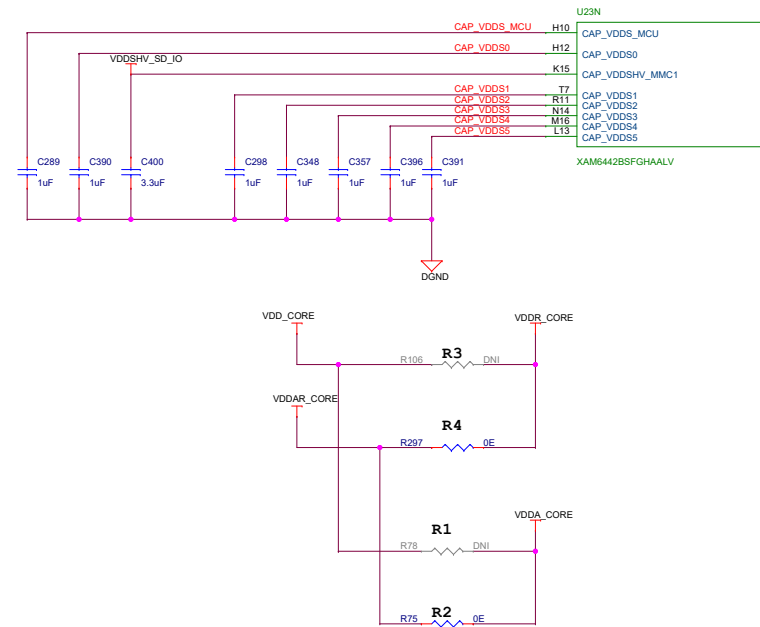
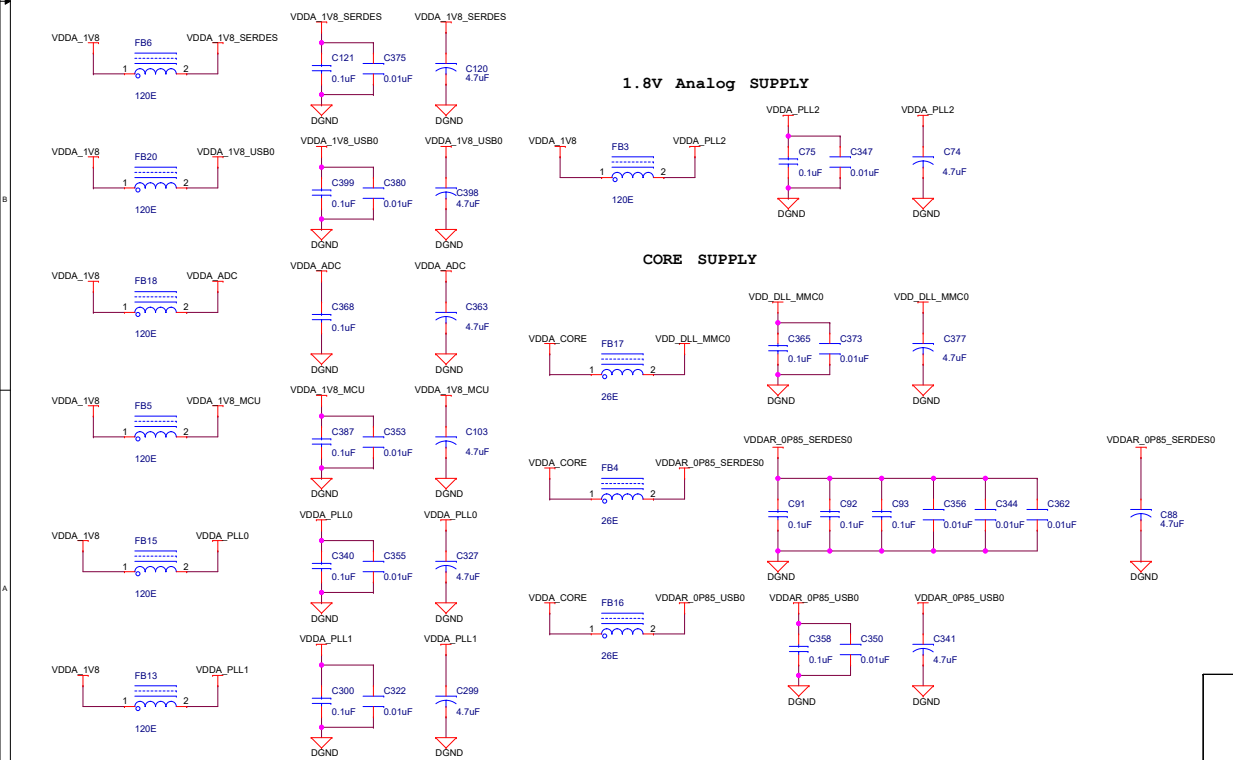
Title I2C TREE

Size	Variant Name = PROC101C(004) TMD564EVM	Rev
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## SoC POWER

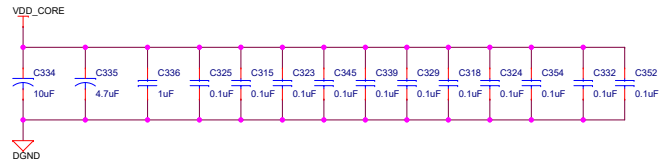


### 1.8V Analog SUPPLY

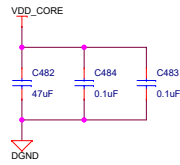


CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

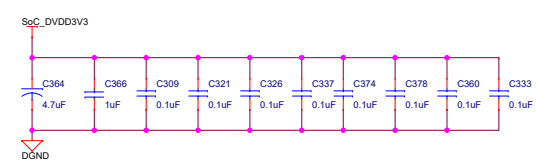
## SoC POWER Decaps



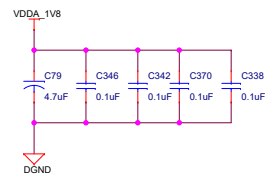
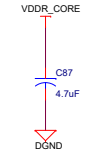
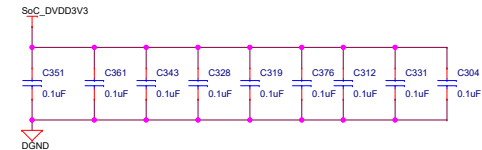
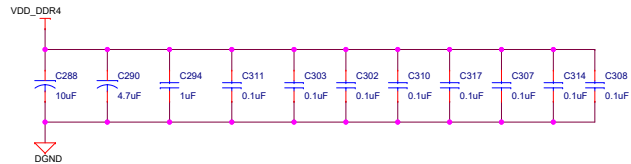
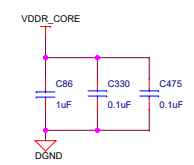
Place one 0.1uF cap near each Pin



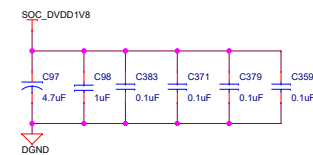
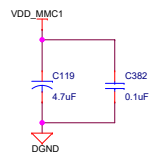
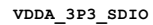
To place after current sense  
resistor on VDD\_CORE plane



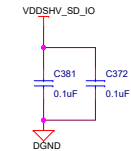
Place one 0.1uF cap near each Pin



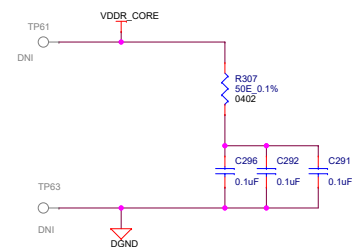
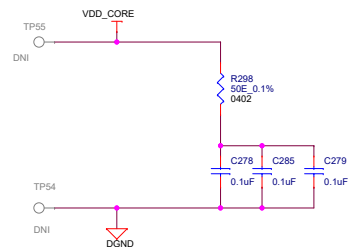
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin



## Core & Array Core Supply Kelvin Sensing



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Title	SOC POWER CAPS
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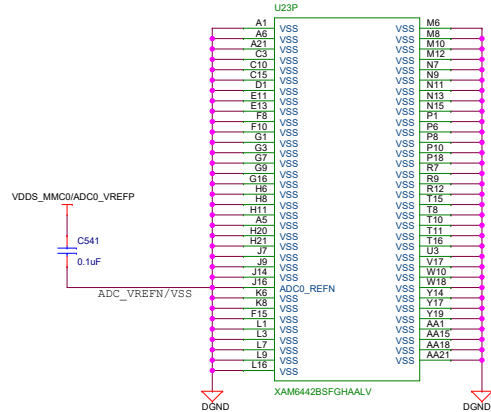
Size	Variant Name = PROC101C(004) TMDS64EVM
C	

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Rev
E2

SoC POWER - VSS

CAD Note:  
Place CAP C541  
between pins  
J15 and J16



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Title SOC VSS

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U23G				
D2	D0R0_A0	D0R0_DM0	B2	DDR_LDM
C5	D0R0_A1	D0R0_DM1	M2	DDR_UDM
D4	D0R0_A2			
F2	D0R0_A3	D0R0_D00	A3	DDR_D00
D0	D0R0_A4	D0R0_D01	A2	DDR_D05
J2	D0R0_A5	D0R0_D02	B5	DDR_D04
L5	D0R0_A6	D0R0_D03	A4	DDR_D01
J3	D0R0_A7	D0R0_D04	B3	DDR_D03
J4	D0R0_A8	D0R0_D05	C4	DDR_D06
K3	D0R0_A9	D0R0_D06	C2	DDR_D07
D0	D0R0_A10	D0R0_D07	B6	DDR_D02
K4	D0R0_A11	D0R0_D08	N5	DDR_D08
M5	D0R0_A12	D0R0_D09	L4	DDR_D015
K4	D0R0_A13	D0R0_D010	L2	DDR_D014
		D0R0_D011	M3	DDR_D010
G4	D0R0_BA0	D0R0_D012	N4	DDR_D09
G5	D0R0_BA1	D0R0_D013	N3	DDR_D012
		D0R0_D014	M4	DDR_D011
G2	D0R0_BG0	D0R0_D015	N2	DDR_D013
H3	D0R0_BG1			
		D0R0_DQ00	C1	DDR_LDQS_P
		D0R0_DQ00_N		
		D0R0_DQ01	N1	DDR_UDQS_P
F1	D0R0_CK0	D0R0_DQ01_N	M1	DDR_UDQS_N
E1	D0R0_CK0_N			
F4	D0R0_CKE0			
F3	D0R0_CKE1			
E3	D0R0_CS0_N			
E4	D0R0_CS1_N			
E5	D0R0_ODT0			
F5	D0R0_ODT1			
H2	D0R0_ACT_N			
H1	D0R0_ALERT_N			
H5	D0R0_CAL0			
J5	D0R0_CAS_N			
K5	D0R0_PAR			
F6	D0R0_RAS_N			
D5	D0R0_RESETO_N			
H4	D0R0_WE_N			

XAM6442BSFGHAAVL

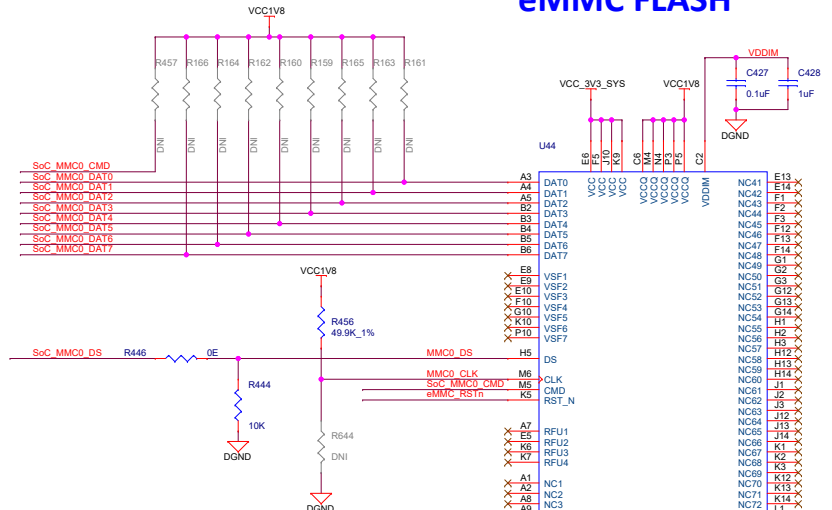
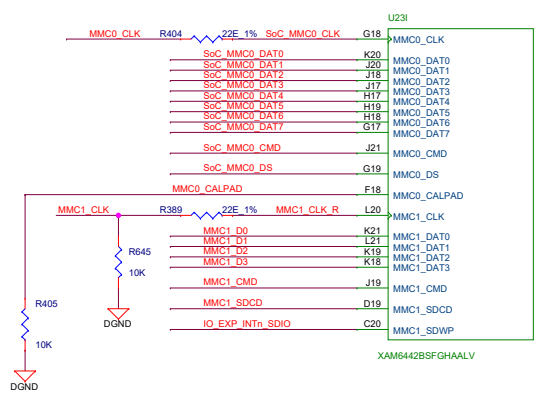
# TERMINATION

The diagram illustrates the termination and signal routing for a DDR4 memory module. It shows a differential pair of DDR4 signals (DDR\_CLKP, DDR\_CLKN) being terminated to VDD\_DDR4 and VDD\_DDR4 with 39.2E-1 ohm resistors. The signals are then routed through a series of 39.2E-1 ohm resistors to a series of capacitors (C248, C244, C251, C267, C64, C61, C246, C254, C264, C63, C62, C60, C59) connected to VDD\_DDR4. The signals are also routed through a series of 39.2E-1 ohm resistors to a series of capacitors (C248, C244, C251, C267, C64, C61, C246, C254, C264, C63, C62, C60, C59) connected to VDD\_DDR4. The signals are also routed through a series of 39.2E-1 ohm resistors to a series of capacitors (C248, C244, C251, C267, C64, C61, C246, C254, C264, C63, C62, C60, C59) connected to VDD\_DDR4. The signals are also routed through a series of 39.2E-1 ohm resistors to a series of capacitors (C248, C244, C251, C267, C64, C61, C246, C254, C264, C63, C62, C60, C59) connected to VDD\_DDR4.

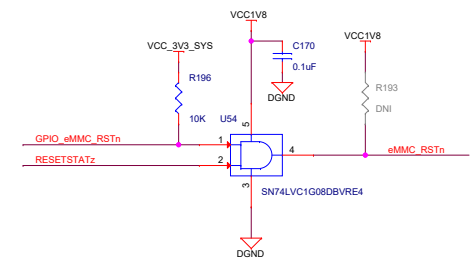


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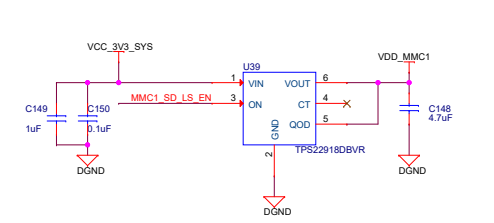
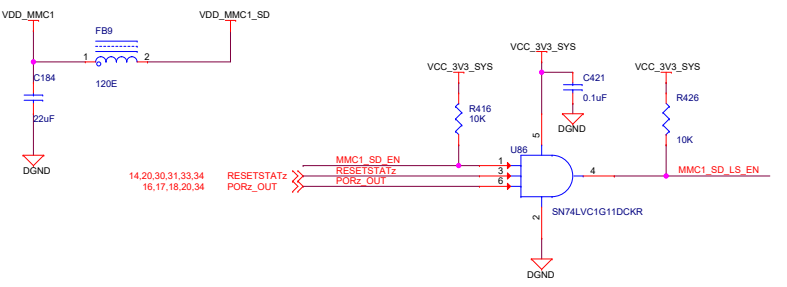
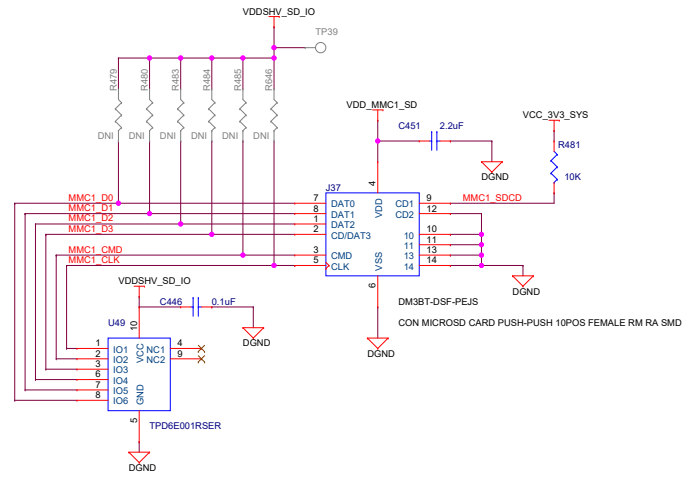
# eMMC FLASH



## eMMC FLASH RESET



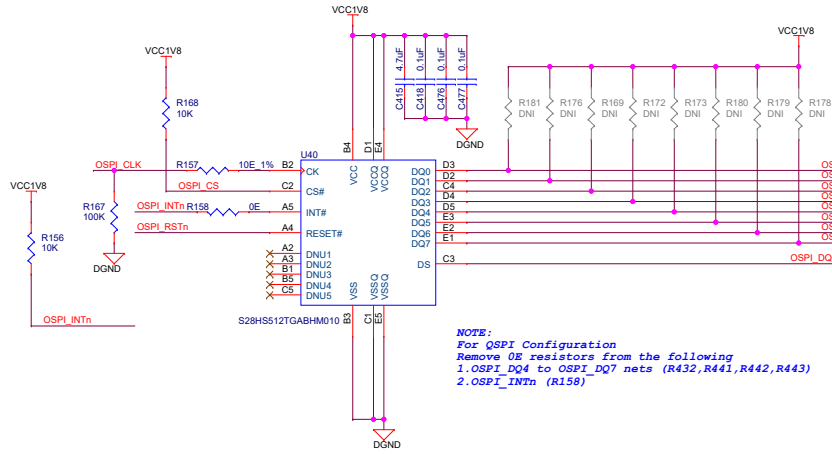
# SD CARD INTERFACE



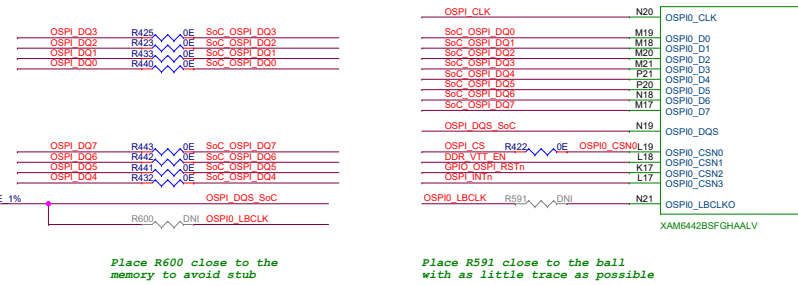
## Off Page Connections

From 4	33	IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
To IO Expander	33	GPIO_eMMC_RSTn	GPIO_eMMC_RSTn
	33	MMC1_SD_EN	MMC1_SD_EN

## OSPI FLASH

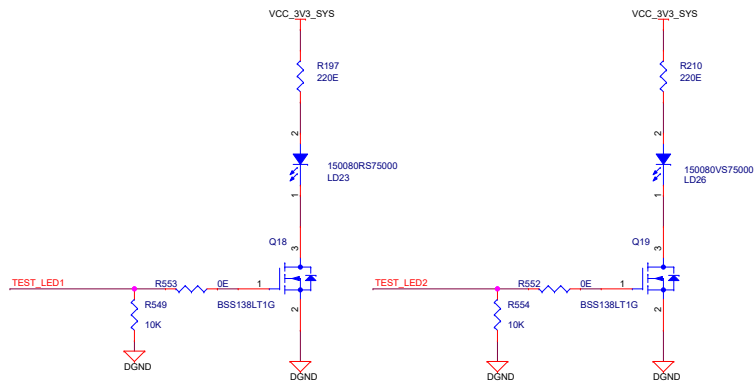


## SOC OSPI INTERFACE

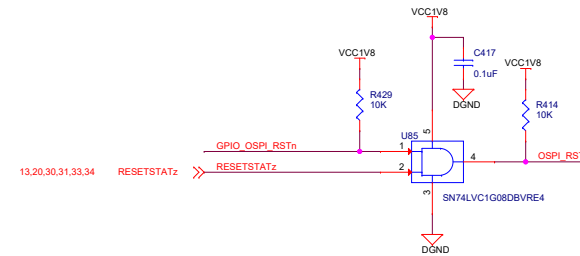


To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	Mount R601 & R592
DNI R601 & R592	DNI R591 & R600

## USER TEST LED



## OSPI FLASH RESET



### Off Page Connections

TEST_LED1	TEST_LED1	33
TEST_LED2	TEST_LED2	34
DDR_VTT_EN	DDR_VTT_EN	33

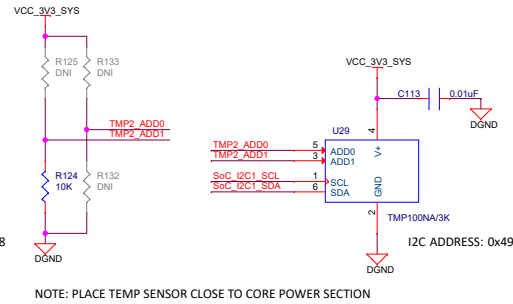
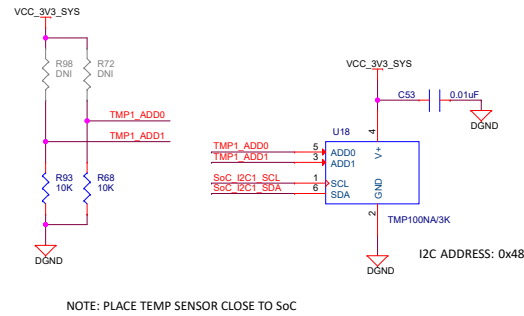
To Level Translator

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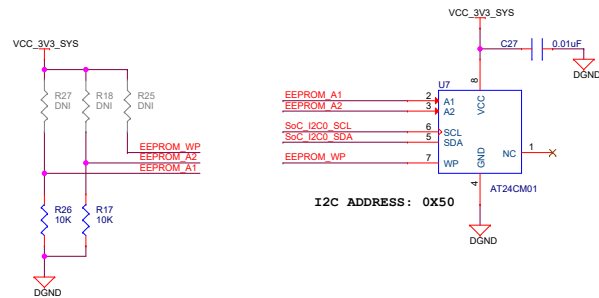
Title		OSPI	
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## TEMPERATURE SENSOR

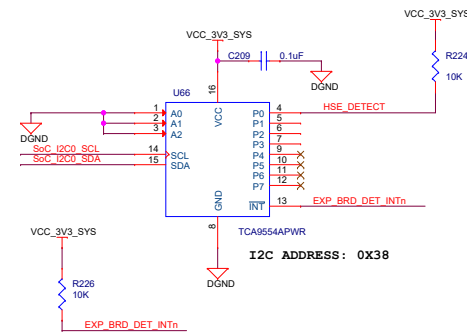


SoC\_I2C1\_SCL DNI TP25  
SoC\_I2C1\_SDA DNI TP27

## BOARD ID EEPROM



## BOARD PRESENCE DETECT CIRCUIT



### Off Page Connections

HSE_DETECT	←	HSE_DETECT	27
SoC_I2C1_SDA	↔	SoC_I2C1_SDA	19,21,29,30,31,32,33
SoC_I2C1_SCL	↔	SoC_I2C1_SCL	19,21,29,30,31,32,33
SoC_I2C0_SDA	↔	SoC_I2C0_SDA	27,29,33
SoC_I2C0_SCL	↔	SoC_I2C0_SCL	27,29,33

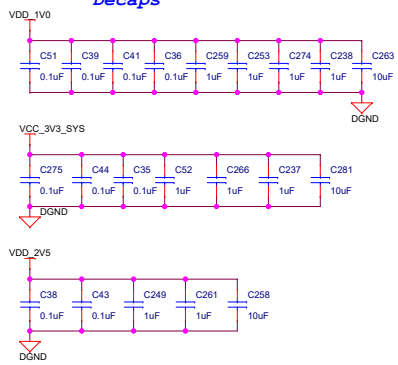
Designed for TI by Mistral Solutions Pvt Ltd



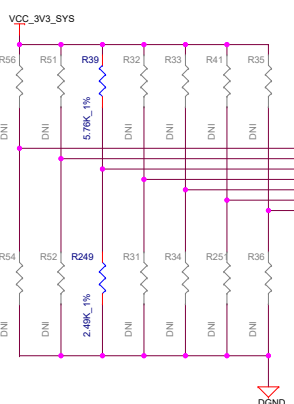
Title EEPROM, PRESENCE DETECTION & TEMP SENSOR

Size	Variant Name = PROC101C(004) TMD564EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 15 of 40

## Decaps

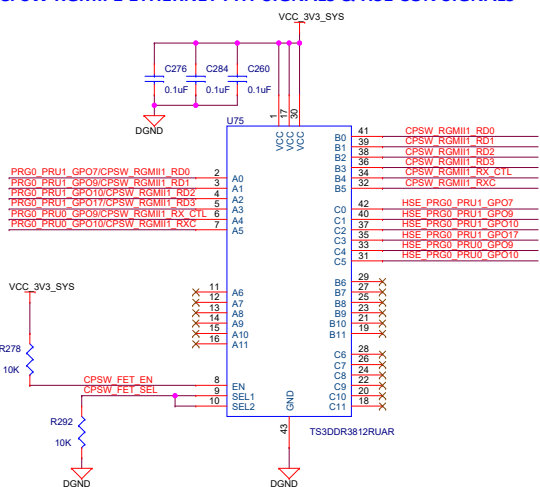


## STRAPPING RESISTORS

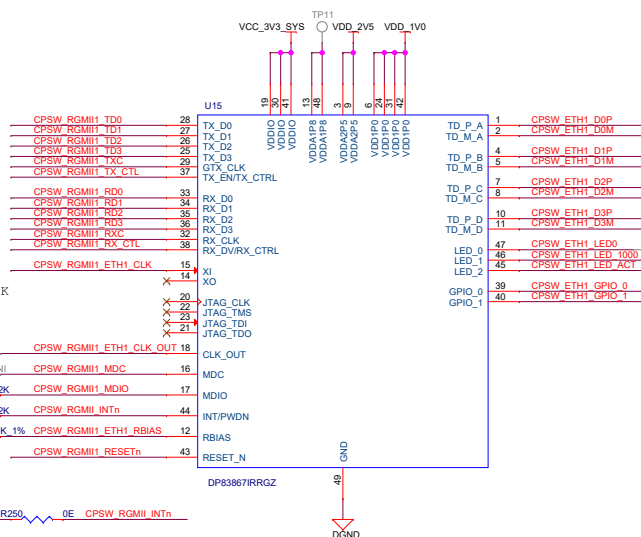


```
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx & Rx Clock Skew = 2.0ns
```

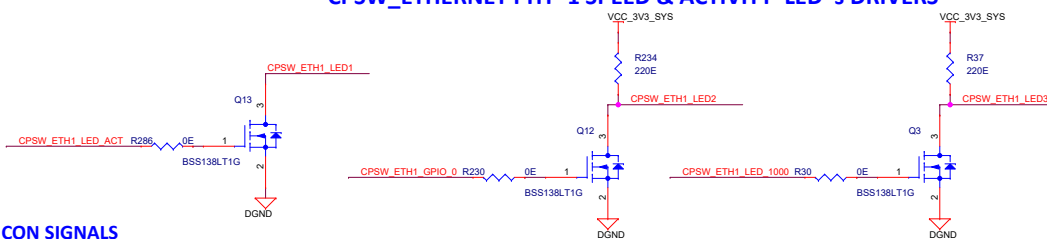
## CPSW RGMII 1 ETHERNET PHY SIGNALS & HSE CON SIGNALS



## CPSW RGMII 1 - PHY



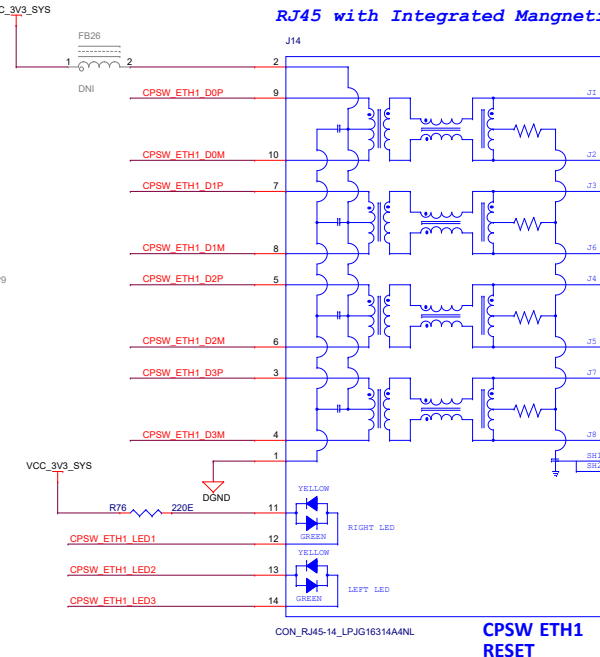
## CPSW\_ETHERNET PHY- 1 SPEED & ACTIVITY LED 's DRIVERS



TS3DDR3812RUAR Truth Table

EN	SEL1	SEL2	FUNCTION
L	X	X	A0 to A11, B0 to B11, and C0 to C11 are Hi-Z
H	L	L	A0 to A5 = B0 to B5 and A6 to A11 = B6 to B11
H	L	H	A0 to A5 = B0 to B5 and A6 to A11 = C6 to C11
H	H	L	A0 to A5 = C0 to C5 and A6 to A11 = B6 to B11
H	H	H	A0 to A5 = C0 to C5 and A6 to A11 = C6 to C11

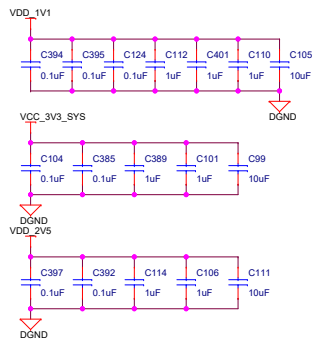
### RJ45 with Integrated Magnetics



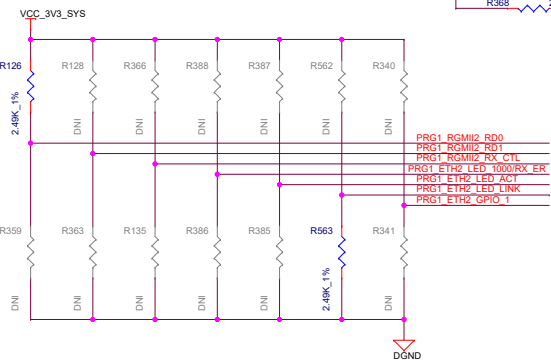
### Off Page Connections

[illegible]

## Decaps

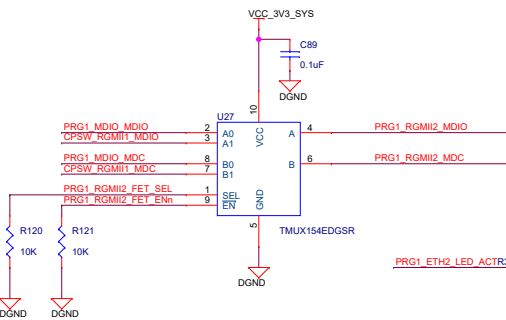


## STRAPPING RESISTORS



PHY ADDRESS = 00011  
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X  
RGMII to Copper (1000BaseT/100Base-TX/10Base-T)

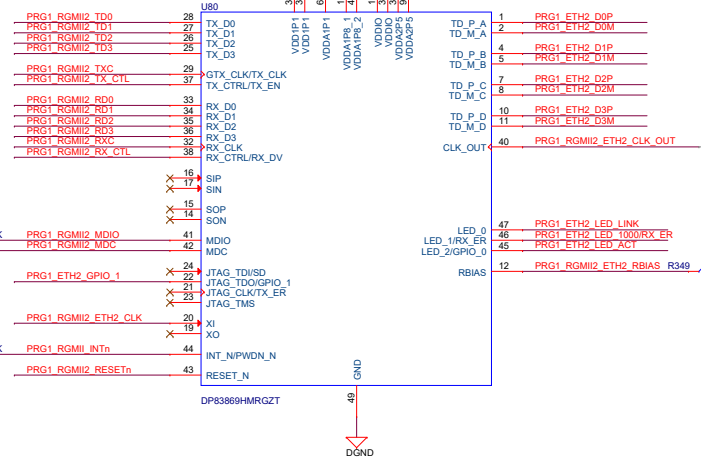
## PRG1 MDC/MDIO FET SWITCH



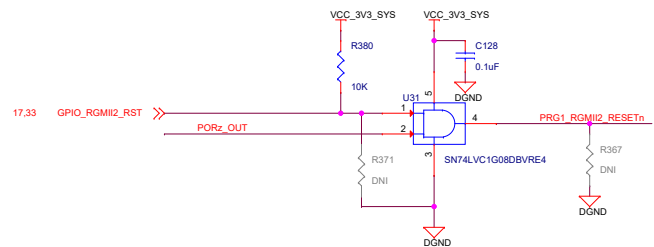
TMUX154EDGSR Truth Table

SEL	EN	FUNCTION
X	H	Decoupled
L	L	A = A0 B = B0
H	L	A = A1 B = B1

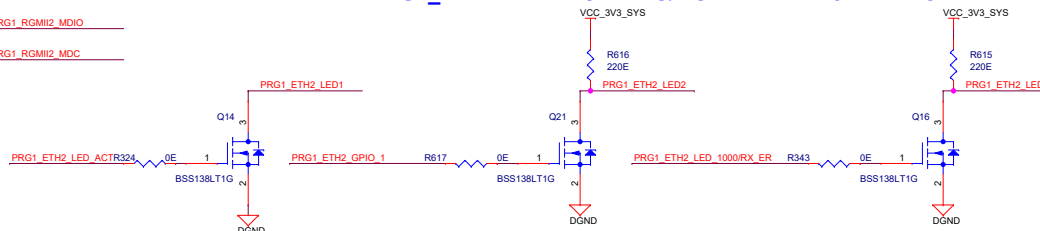
## ICSSG1 - RGMII 2



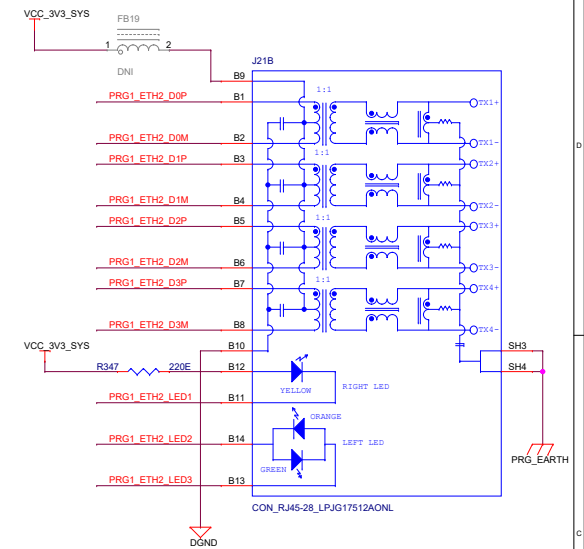
## PRG1 ETH2 RESET



## PRG1\_ETHERNET - 2 SPEED &amp; ACTIVITY LED's DRIVERS



## Dual RJ45 CON With Integrated Magnetics



## Off Page Connections

To Processor	16,18,34	PRG1_RGMII2_INTn	PRG1_RGMII2_INTn
	27	PRG1_RGMII2_RD0	PRG1_RGMII2_RD0
	27	PRG1_RGMII2_RD1	PRG1_RGMII2_RD1
	27	PRG1_RGMII2_RD2	PRG1_RGMII2_RD2
	27	PRG1_RGMII2_RD3	PRG1_RGMII2_RD3
	27	PRG1_RGMII2_RXC	PRG1_RGMII2_RXC
	27	PRG1_RGMII2_RX_CTL	PRG1_RGMII2_RX_CTL
	27	PRG1_ETH2_LED_LINK	PRG1_ETH2_LED_LINK
	27	PRG1_ETH2_LED_1000RX_ER	PRG1_ETH2_LED_1000RX_ER
From Processor	27	PRG1_RGMII2_TD0	PRG1_RGMII2_TD0
	27	PRG1_RGMII2_TD1	PRG1_RGMII2_TD1
	27	PRG1_RGMII2_TD2	PRG1_RGMII2_TD2
	27	PRG1_RGMII2_TD3	PRG1_RGMII2_TD3
	27	PRG1_RGMII2_TXC	PRG1_RGMII2_TXC
	27	PRG1_RGMII2_TX_CTL	PRG1_RGMII2_TX_CTL
	13,16,18,20,34	PORz_OUT	PORz_OUT
	18,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	18,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From CPSW SW	16,27	CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
	16,27	CPSW_RGMII1_MDC	CPSW_RGMII1_MDC
From IO Expander	17,33	GPIO_RGMII2_RST	GPIO_RGMII2_RST
	33	PRG1_RGMII2_FET_SEL	PRG1_RGMII2_FET_SEL
From Clock Buffer	31	PRG1_RGMII2_ETH2_CLK	PRG1_RGMII2_ETH2_CLK

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Title ICSSG1 RGMII\_2 ETHERNET PHY

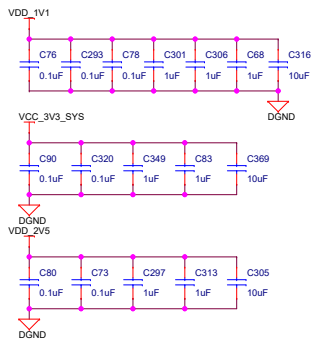
Size Variant Name = PROC101C(004) TMD564EVM  
C  
Date: Thursday, August 18, 2022

Rev  
E2

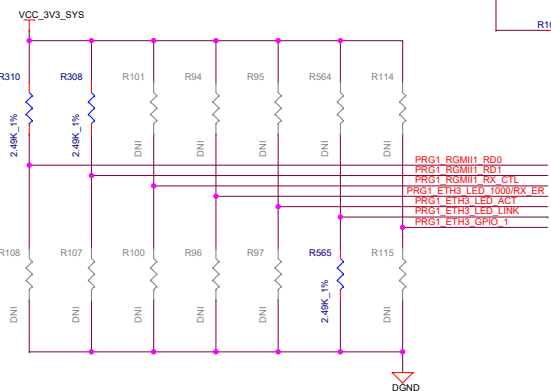
Sheet 17 of 40

# ICSSG1 - RGMII 1

## Decaps

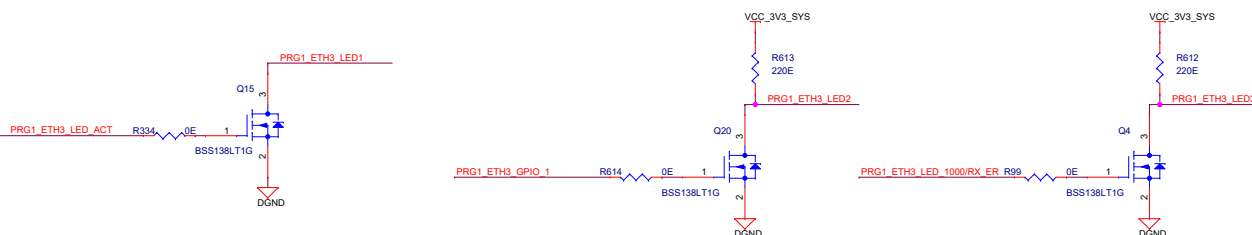


## STRAPPING RESISTORS

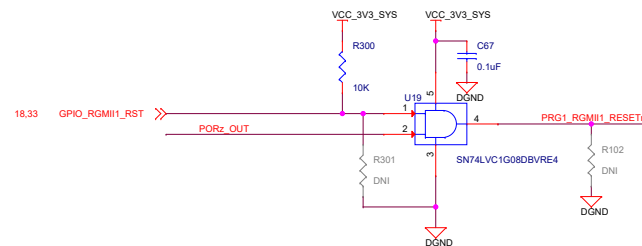


PHY ADDRESS = 01111  
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X  
RGMII to Copper (1000Base-T/100Base-TX/10Base-T)

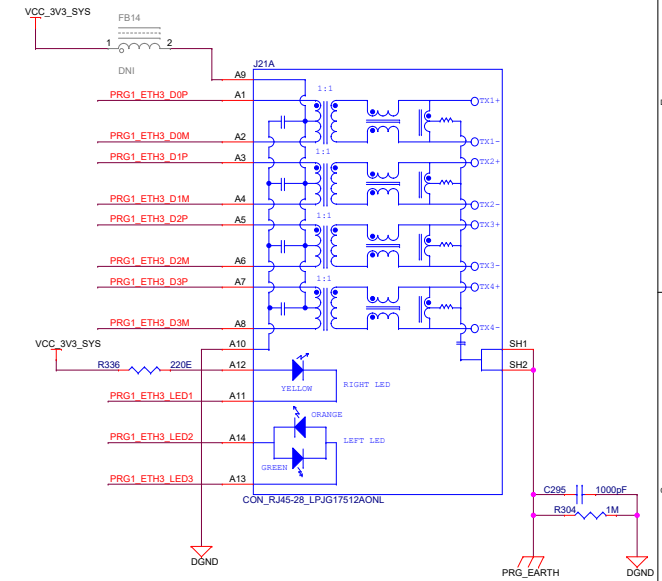
## PRG1\_ETHERNET - 3 SPEED & ACTIVITY LED's DRIVERS



## PRG1 ETH2 RESET



## Dual RJ45 CON With Integrated Magnetics



## Off Page Connections

To Processor	16,17,34	PRG1_RGMII_INTn	PRG1_RGMII_INTn
	27	PRG1_RGMII_RD0	PRG1_RGMII_RD0
	27	PRG1_RGMII_RD1	PRG1_RGMII_RD1
	27	PRG1_RGMII_RD2	PRG1_RGMII_RD2
	27	PRG1_RGMII_RD3	PRG1_RGMII_RD3
	27	PRG1_RGMII_RXC	PRG1_RGMII_RXC
	27	PRG1_RGMII_RX_CTL	PRG1_RGMII_RX_CTL
13,16,17,20,34	PORz_OUT	PORz_OUT	
	27	PRG1_ETH3_LED_LINK	PRG1_ETH3_LED_LINK
27	PRG1_ETH3_LED_1000RX_ER	PRG1_ETH3_LED_1000RX_ER	
From Processor	27	PRG1_RGMII_TD0	PRG1_RGMII_TD0
	27	PRG1_RGMII_TD1	PRG1_RGMII_TD1
	27	PRG1_RGMII_TD2	PRG1_RGMII_TD2
	27	PRG1_RGMII_TD3	PRG1_RGMII_TD3
	27	PRG1_RGMII_TXC	PRG1_RGMII_TXC
	27	PRG1_RGMII_TX_CTL	PRG1_RGMII_TX_CTL
From Processor	17,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	(MDC & MDIO Pins are common to both ICSSG PHY, this to be verified)	17,27	PRG1_MDIO_MDC
From IO Expander	18,33	GPIO_RGMII_RST	GPIO_RGMII_RST
From Clock Buffer	31	PRG1_RGMII_ETH3_CLK	PRG1_RGMII_ETH3_CLK

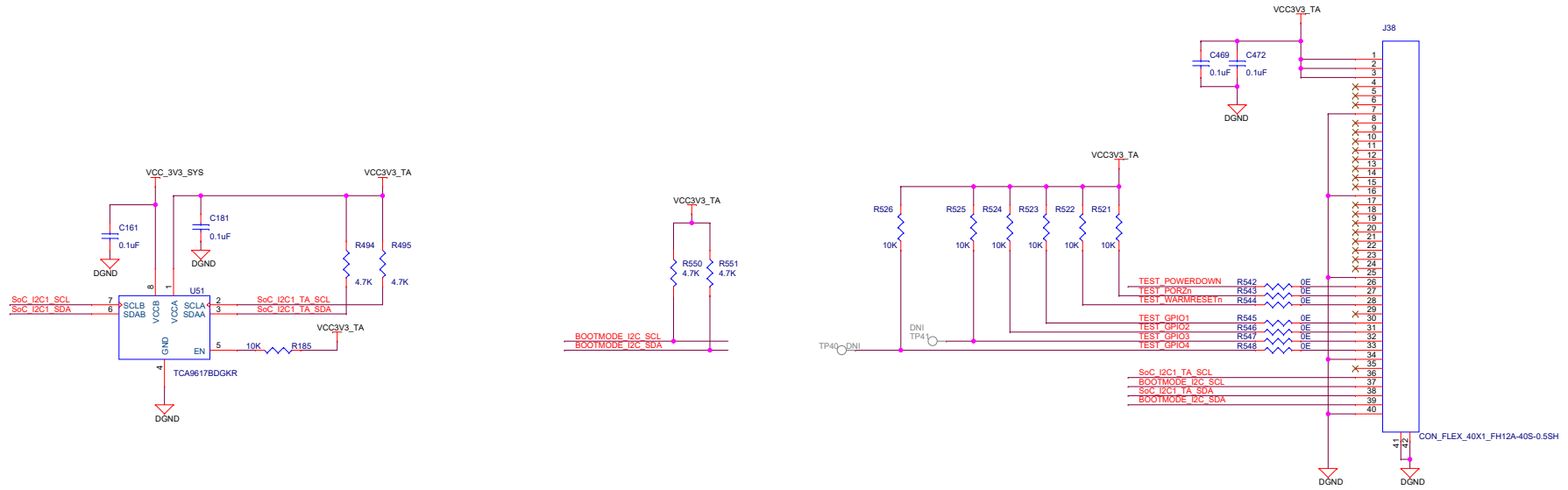
Designed for TI by Mistral Solutions Pvt Ltd



Title ICSSG2 RGMII_1 ETHERNET PHY			
Size	Variant Name = PROC101C(004) TMD564EVM		Rev
C			E2
Date:	Thursday, August 18, 2022	Sheet	18 of 40

# TEST AUTOMATION

## 40-PIN AUTOMATION HEADER



## TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to I/O Expander to Communicate with SoC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

### Off Page Connections

To Processor	15,21,29,30,31,32,33	SoC_I2C1_SCL	SoC_I2C1_SCL
	15,21,29,30,31,32,33	SoC_I2C1_SDA	SoC_I2C1_SDA
To Bootmode Buffer	20	BOOTMODE_I2C_SCL	BOOTMODE_I2C_SCL
	20	BOOTMODE_I2C_SDA	BOOTMODE_I2C_SDA
To Debounce Ckt	35	TEST_PORZn	TEST_PORZn
To High Side SW	37	TEST_POWERDOWN	TEST_POWERDOWN
To Debounce Ckt	35	TEST_WARMRESETn	TEST_WARMRESETn
To IO Expander	35	TEST_GPIO1	TEST_GPIO1
To EN Boot Mode Buffer	33	TEST_GPIO2	TEST_GPIO2
To RST Boot Mode Buffer	20	TEST_GPIO3	TEST_GPIO3
	20	TEST_GPIO4	TEST_GPIO4

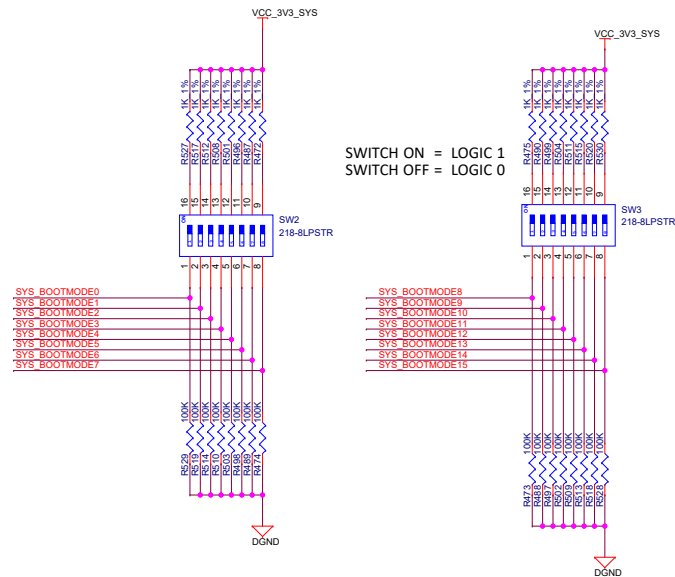
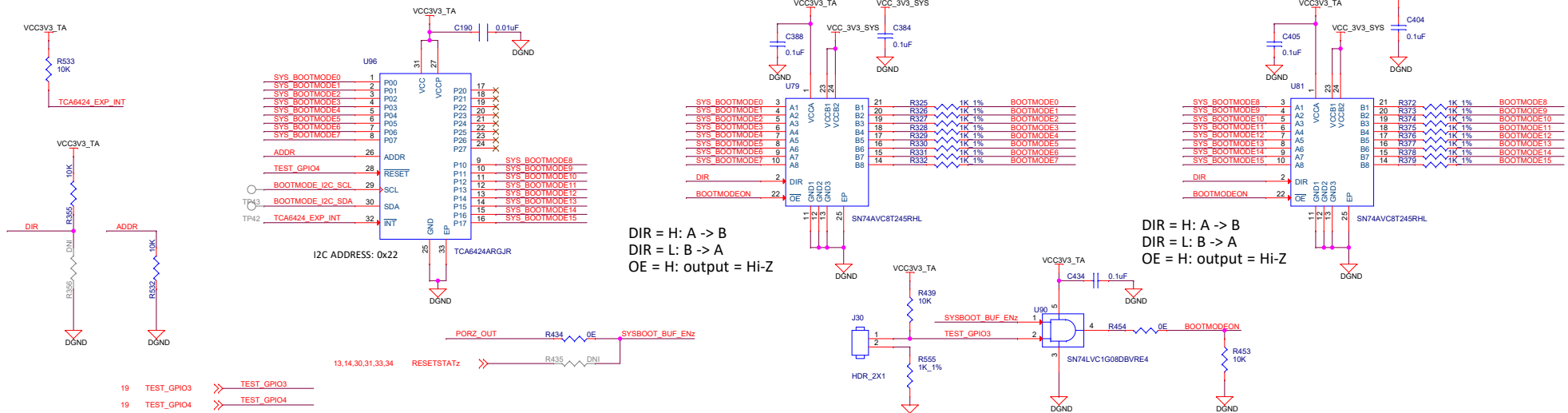
Designed for TI by Mistral Solutions Pvt Ltd



Title TEST AUTOMATION

Size	Variant Name = PROC101C(004) TMD564EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 19 of 40

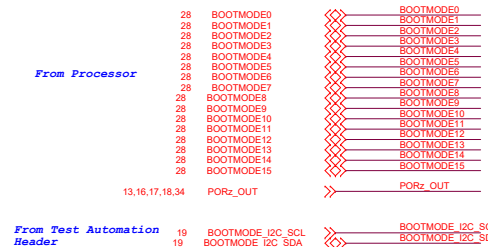
# BOOT MODE BUFFER & SWITCHES



## BOOT MODES SUPPORTED

- OSPI
- MMC1 - SD CARD
- MMC0 - eMMC
- CPSW Ethernet Slave
- USB Host
- USB Device
- UART
- Ethernet

## Off Page Connections



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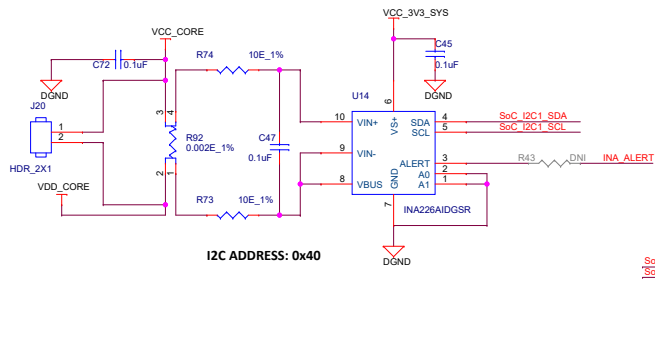


Title BOOT MODE BUFFER & SWITCHES

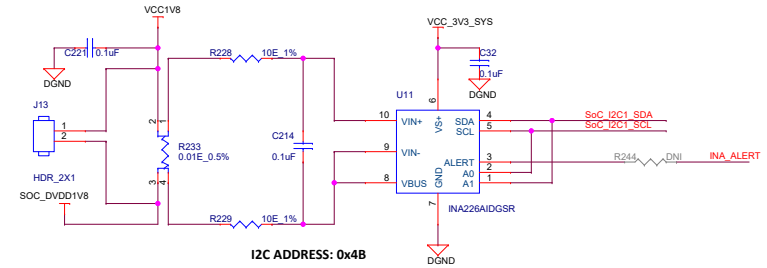
Size	Variant Name = PROC101C(004) TMD564EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 20 of 40

# CURRENT MONITORING DEVICES

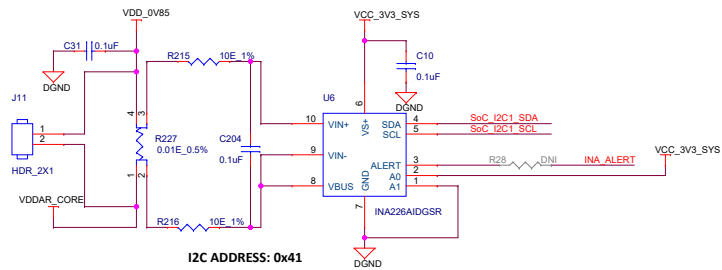
## VDD\_CORE



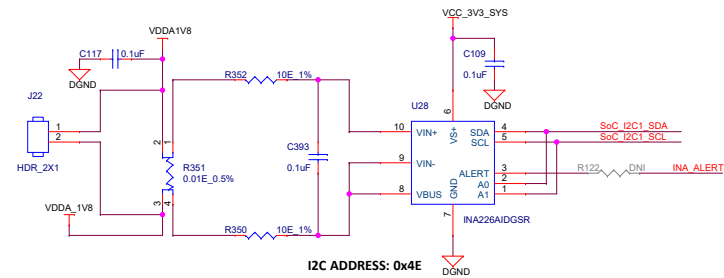
## SoC\_DVDD1V8



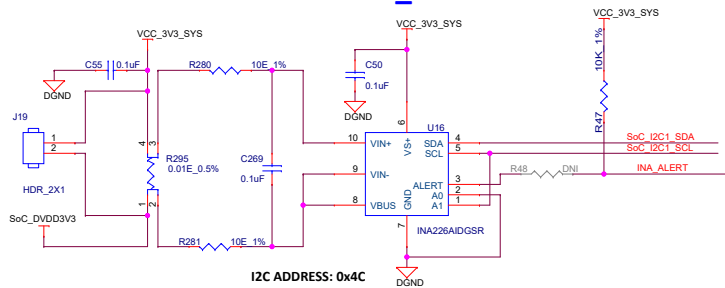
## VDDAR\_CORE



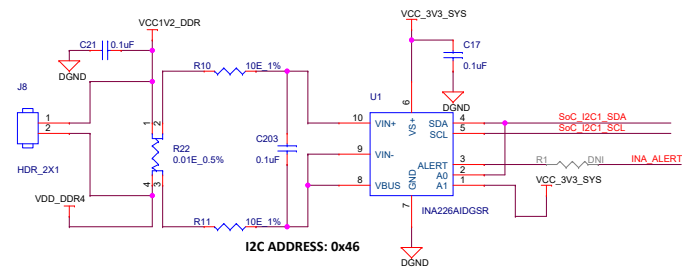
## VDDA\_1V8



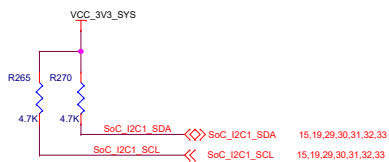
## SoC\_DVDD3V3



## VDD\_DDR4



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_OV85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46



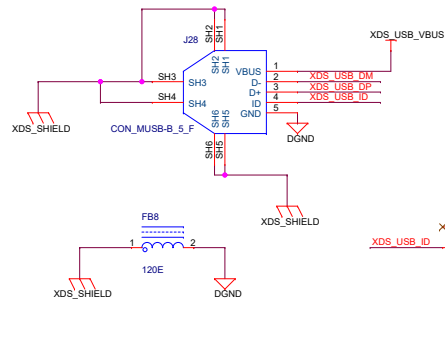
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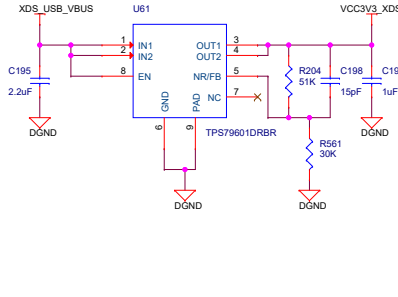
Title CURRENT MONITORING DEVICES

Size	Variant Name = PROC101C(004) TMD564EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 21 of 40

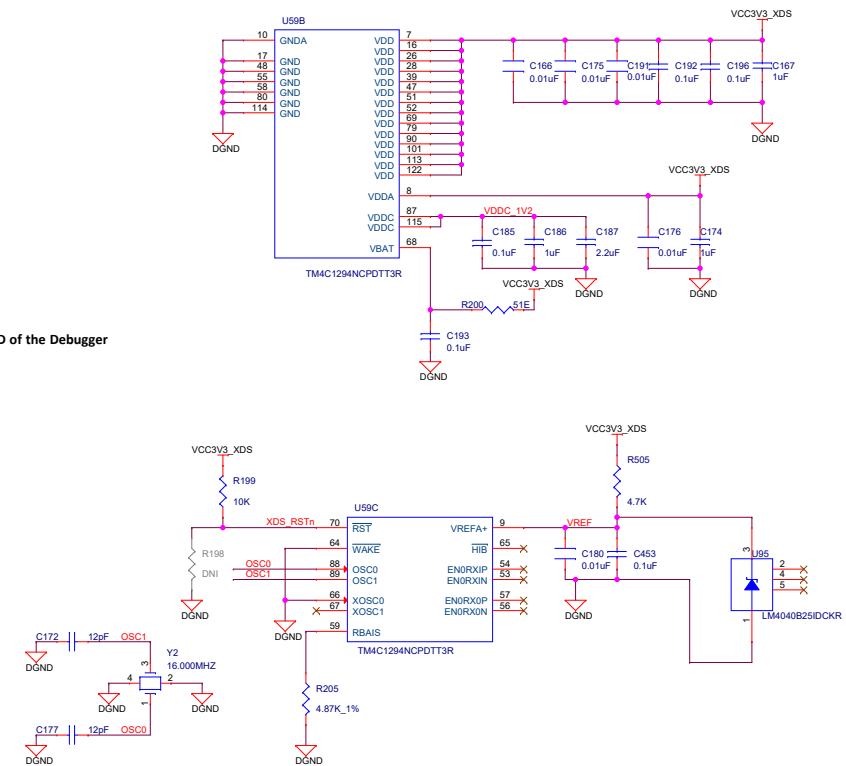
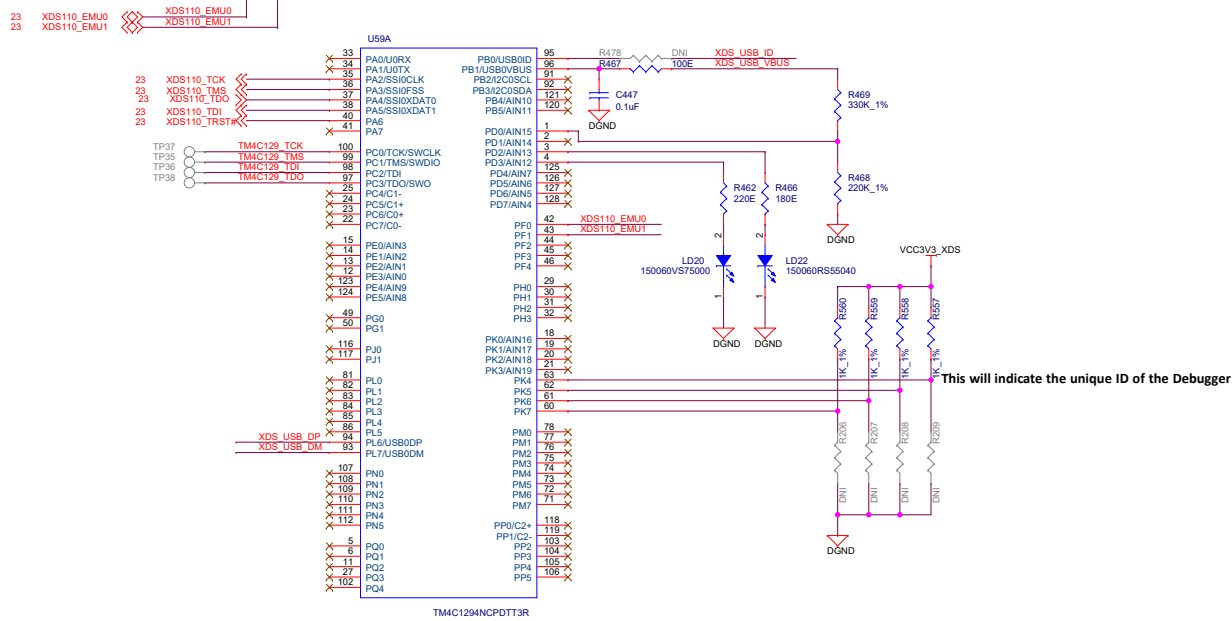
## USB Connector



## XDS110 POWER



## XDS110 DEBUGGER



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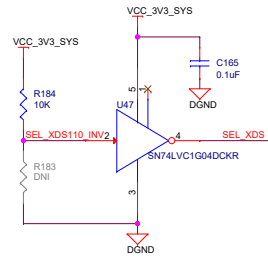
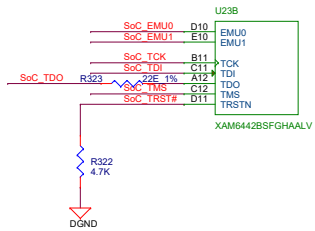


Title XDS110 DEBUGGER

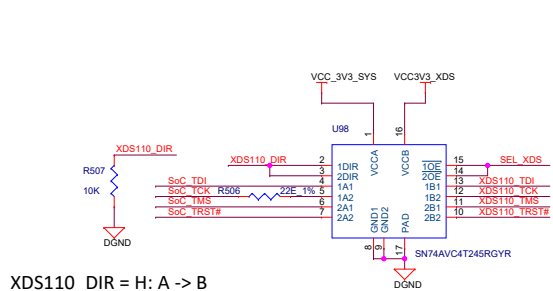
Size	Variant Name = PROC101C(004) TMD564EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 22 of 40

## JTAG BUFFER

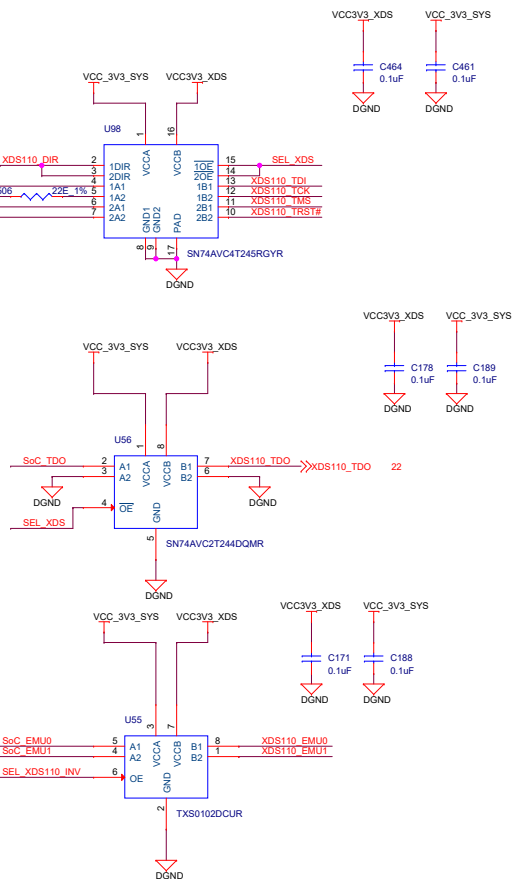
## JTAG SoC SECTION



## BUFFER XDS110

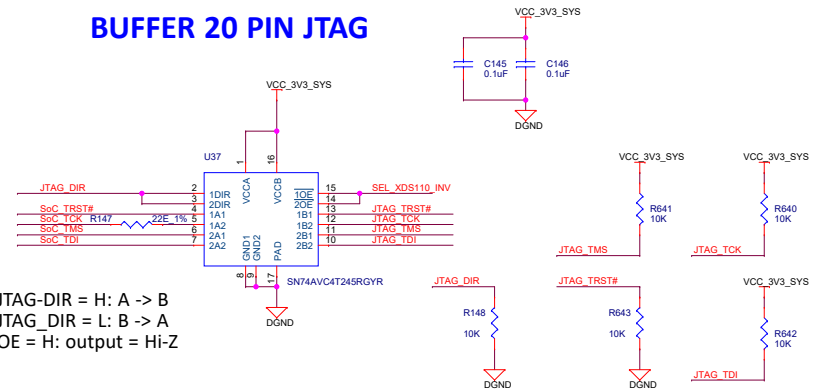


XDS110\_DIR = H: A -> B  
XDS110\_DIR = L: B -> A  
OE = H: output = Hi-Z

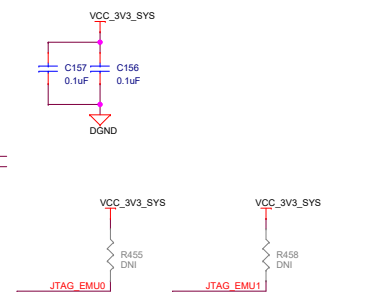
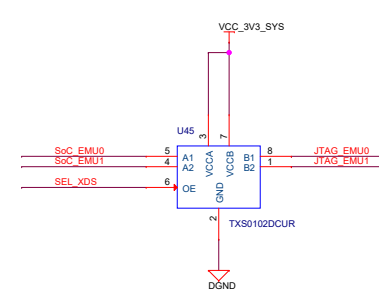
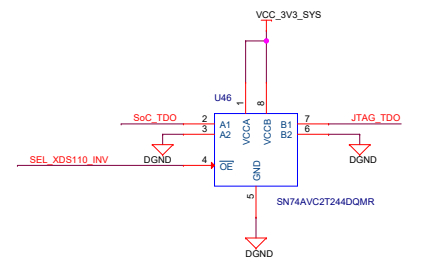


Placement of Buffers U37, U46, U56 and U98 to be changed to reduce Stub length of the JTAG signals. These buffers need to be placed closer to the cTI-20pin connector -J25

## BUFFER 20 PIN JTAG



JTAG-DIR = H: A -> B  
JTAG\_DIR = L: B -> A  
OE = H: output = Hi-Z



### Off Page Connections

24	SEL_XDS110_INV	SEL_XDS110_INV
24	JTAG_EMU0	JTAG_EMU0
24	JTAG_EMU1	JTAG_EMU1
22	XDS110_TDI	XDS110_TDI
22	XDS110_TCK	XDS110_TCK
22	XDS110_TMS	XDS110_TMS
22	XDS110_TRST#	XDS110_TRST#
24	JTAG_TDI	JTAG_TDI
24	JTAG_TCK	JTAG_TCK
24	JTAG_TMS	JTAG_TMS
24	JTAG_TRST#	JTAG_TRST#
24	JTAG_TDO	JTAG_TDO
22	XDS110_EMU0	XDS110_EMU0
22	XDS110_EMU1	XDS110_EMU1

From XDS1100  
Debugger

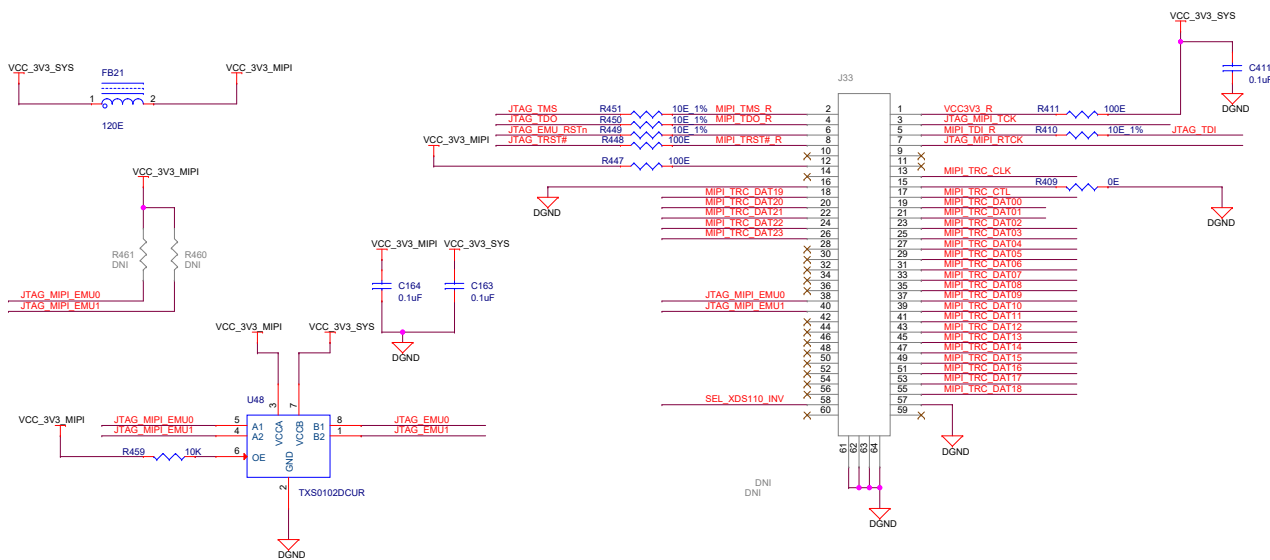
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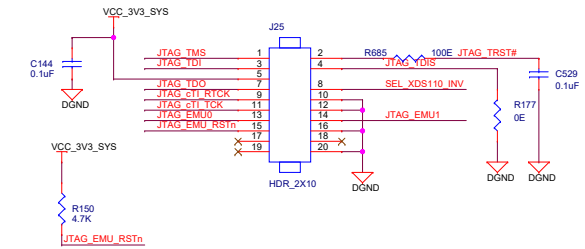
<b>Title</b>	<b>JTAG BUFFER</b>
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Size	Variant Name = PROC101C(004) TMS64EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 23 of 40

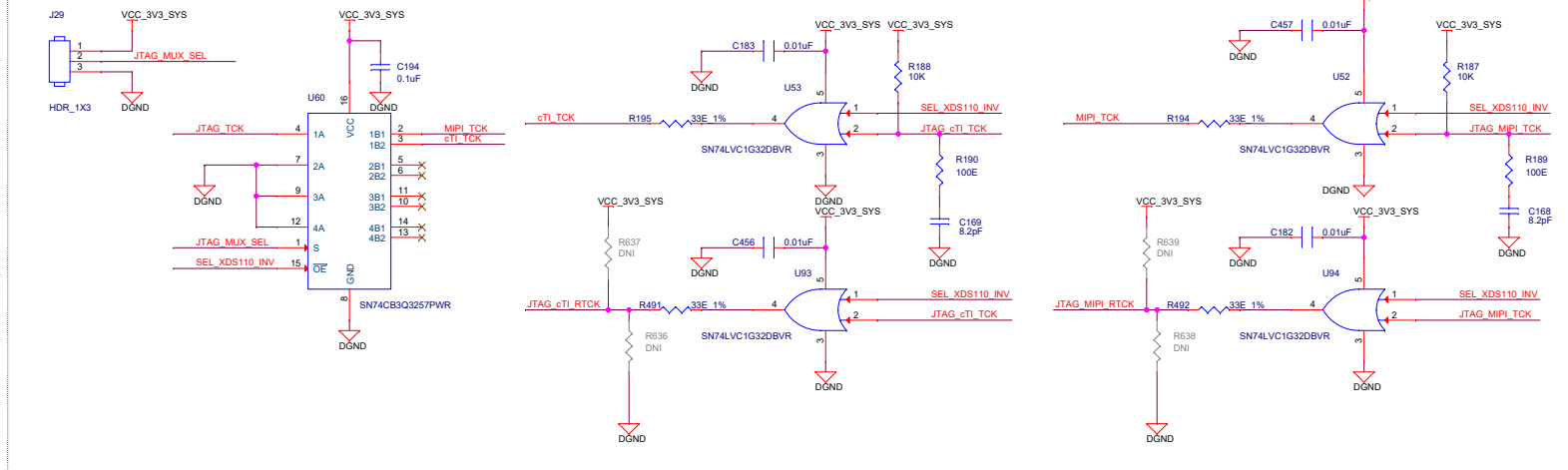
## MIPI 60 PIN CONNECTOR



## JTAG 20 PIN cTI CONNECTOR

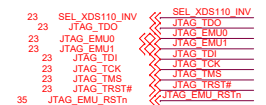


## JTAG CLOCK BUFFER

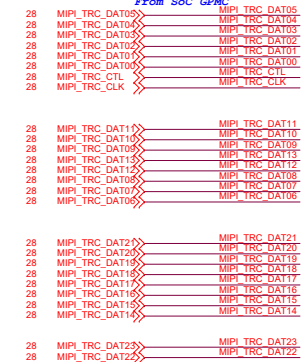


### Off Page Connections

From JTAG Buffer



From SoC GPMC



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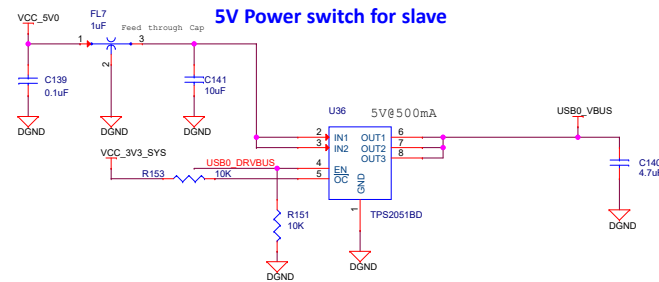
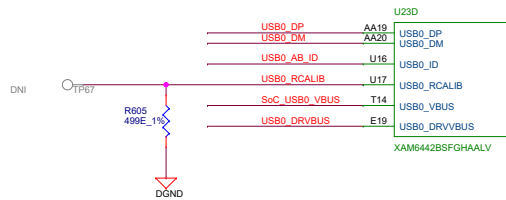
Title	MIPI 60 PIN CONNECTOR
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Size	Variant Name = PROC101C(004) TMD564EVM
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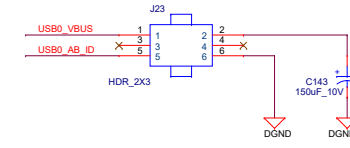
Date:	Thursday, August 18, 2022	Sheet	24	of	40
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Rev
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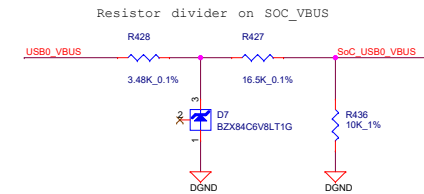
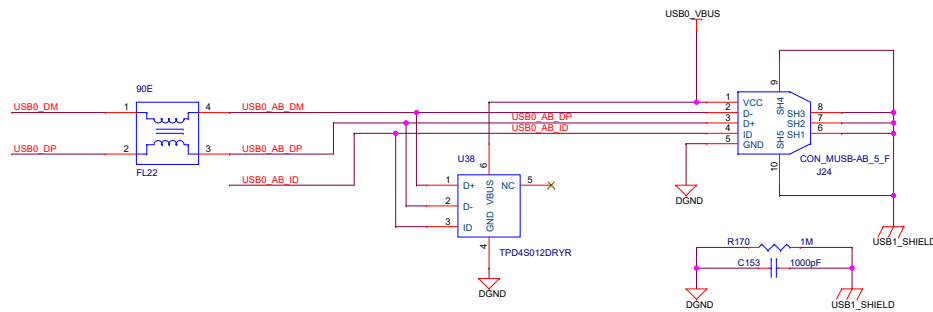
# USB 2.0 INTERFACE



2X3 header to enable bulk capacitance on USB0\_VBUS in host mode and to ground USB0\_AB\_ID pin, if a non standard cable is used



## Micro USB 2.0 AB Connector



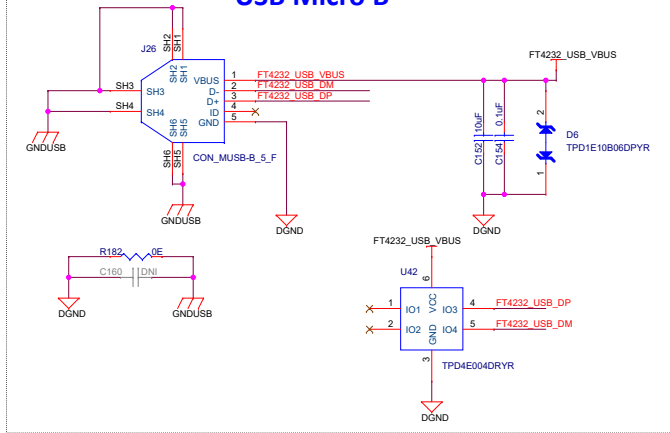
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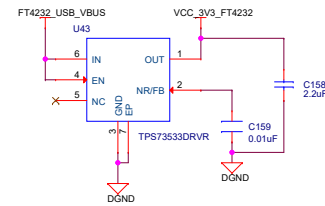
Title USB 2.0 INTERFACE

Size	Variant Name = PROC101C(004) TMD684EVM	Rev
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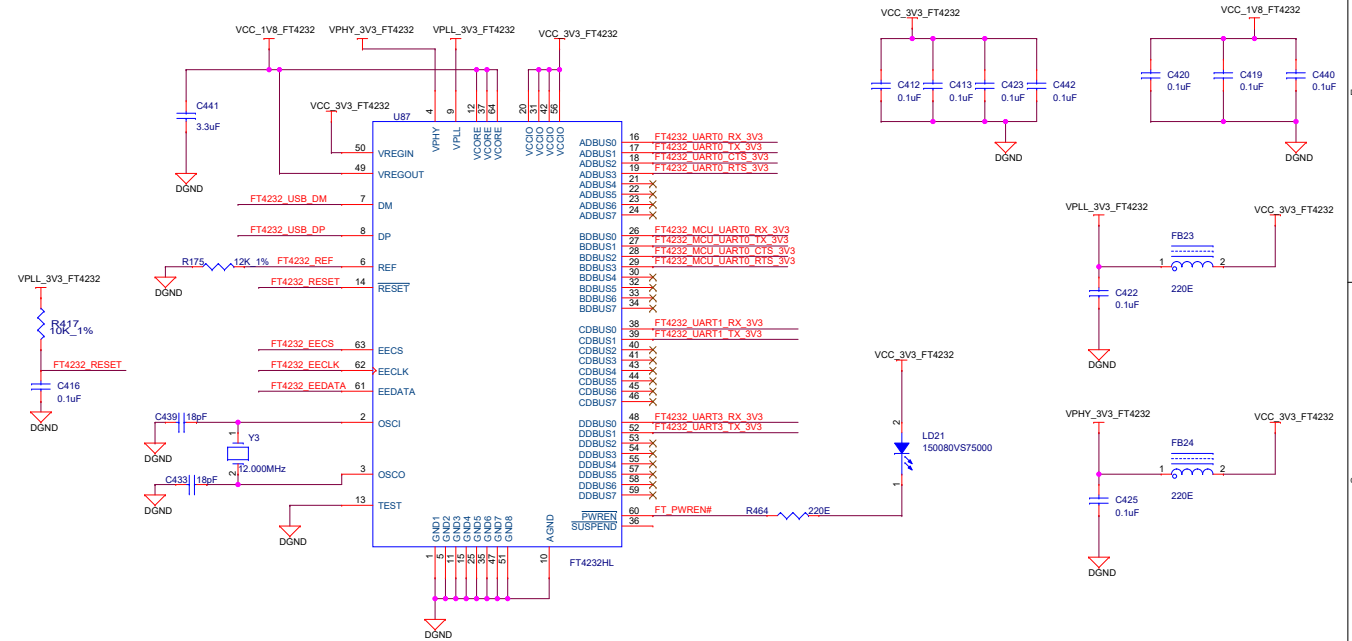
## USB Micro B



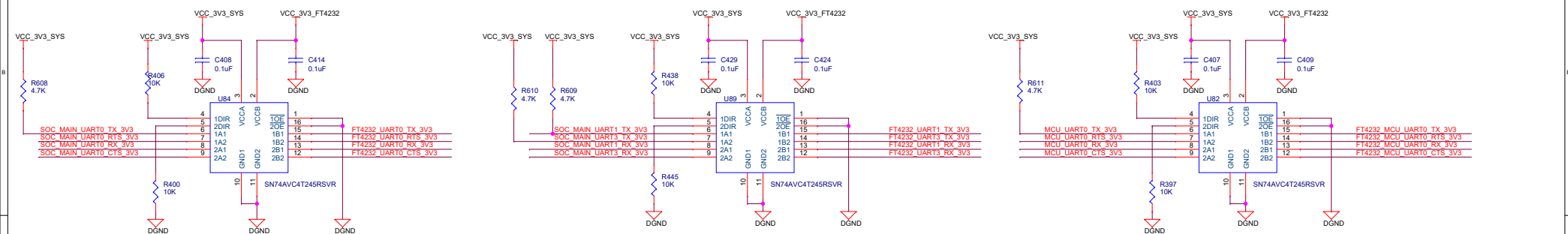
## FT4232: 5V to 3.3V@500mA LDO



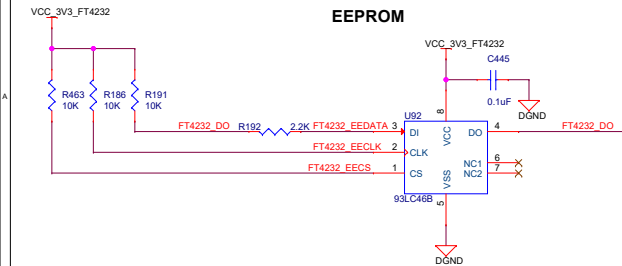
## FT4232 UART



## FT4232 LEVEL TRANSLATOR



## EEPROM



## Off Page Connections

SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3	29
SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3	29
SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3	29
SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3	29
MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	34
MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	34
MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	34
MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	34
SOC_MAIN_UART1_RX_3V3	SOC_MAIN_UART1_RX_3V3	29
SOC_MAIN_UART1_TX_3V3	SOC_MAIN_UART1_TX_3V3	29
SOC_MAIN_UART1_RTS_3V3	SOC_MAIN_UART1_RTS_3V3	29
SOC_MAIN_UART1_CTS_3V3	SOC_MAIN_UART1_CTS_3V3	29

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Title FT4232 UART to USB BRIDGE

Size	Variant Name = PROC101C(004) TMD564EVM	Rev
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**J18**

1 2

PRG1 IEPO\_EDC\_SYNC\_OUT0

HDR\_2X1

DGND

**J17**

1 2

PRG1 IEPO\_EDC\_LATCH\_IN0

HDR\_2X1

DGND

**J16**

1 2

PRG1 IEPO\_EDC\_SYNC\_OUT2

HDR\_2X1

DGND

**J15**

1 2

PRG1 IEPO\_EDC\_LATCH\_IN1

HDR\_2X1

DGND

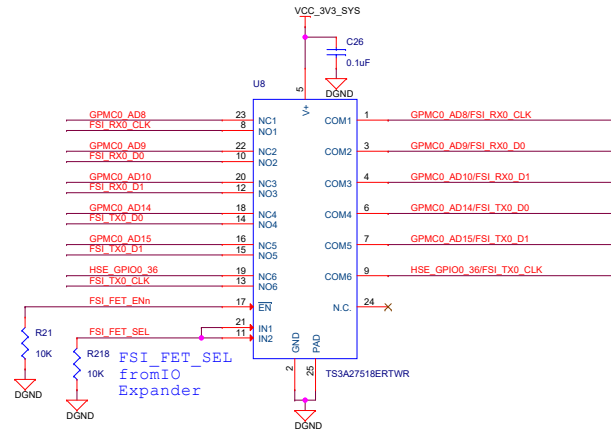
[illegible]

To Presence Detect Buffer	15	HSE_DETECT	<<	HSE_DETECT
From Processor GPMC	28	GPMCO_CSn1	<<	GPMCO_CSn1
	28	GPMCO_CSn2	<<	GPMCO_CSn2
	28	GPMCO_CSn3	<<	GPMCO_CSn3
	28	GPMCO_DIR	<<	GPMCO_DIR
From FSI mux	28	GPMCO_A08	<<	GPMCO_A08
	28	GPMCO_A09	<<	GPMCO_A09
	28	GPMCO_A10	<<	GPMCO_A10
	28	GPMCO_A11	<<	GPMCO_A11
	28	GPMCO_A12	<<	GPMCO_A12
	28	GPMCO_A13	<<	GPMCO_A13
From Processor GPMC resistor muxed with MIPI	28	HSE_GPI00_36	<<	HSE_GPI00_36
	28	GPMCO_A00	<<	GPMCO_A00
	28	GPMCO_A01	<<	GPMCO_A01
	28	GPMCO_A02	<<	GPMCO_A02
	28	GPMCO_A03	<<	GPMCO_A03
	28	GPMCO_A04	<<	GPMCO_A04
	28	GPMCO_A05	<<	GPMCO_A05
	28	GPMCO_A06	<<	GPMCO_A06
	28	GPMCO_A07	<<	GPMCO_A07
	28	GPMCO_A08	<<	GPMCO_A08
	28	GPMCO_A09	<<	GPMCO_A09
	28	GPMCO_A10	<<	GPMCO_A10
	28	GPMCO_A11	<<	GPMCO_A11
	28	GPMCO_A12	<<	GPMCO_A12
	28	GPMCO_A13	<<	GPMCO_A13
	28	HSE_GPI00_31	<<	HSE_GPI00_31
	28	HSE_GPI00_32	<<	HSE_GPI00_32
	28	HSE_GPI00_33	<<	HSE_GPI00_33
	28	HSE_GPI00_34	<<	HSE_GPI00_34
	28	HSE_GPI00_35	<<	HSE_GPI00_35
	28	HSE_GPI00_36	<<	HSE_GPI00_36
	28	HSE_GPI00_37	<<	HSE_GPI00_37
	28	HSE_GPI00_38	<<	HSE_GPI00_38
	28	HSE_GPI00_39	<<	HSE_GPI00_39
From Processor	34	MCU_PORz	<<	MCU_PORz
	34,35	MCU_RESETz	<<	MCU_RESETz
	34	MCU_RESETStz	<<	MCU_RESETStz
	29	HSE_MCAN0_RXUART4_TXD	<<	HSE_MCAN0_RXUART4_TXD
	29	HSE_MCAN0_TXUART4_RXD	<<	HSE_MCAN0_TXUART4_RXD
	29	HSE_MCAN1_TXI2C3_SCL	<<	HSE_MCAN1_TXI2C3_SCL
	29	HSE_MCAN1_TXI2C3_SCL	<<	HSE_MCAN1_TXI2C3_SCL
	29	SOC_SPI1_CLK	<<	SOC_SPI1_CLK
	29	SOC_SPI1_MOSI	<<	SOC_SPI1_MOSI
	29	SOC_SPI1_MISO	<<	SOC_SPI1_MISO
	29	SOC_SPI1_CS1	<<	SOC_SPI1_CS1
	15,29,33	SOC_I2C0_SCL	<<	SOC_I2C0_SCL
	15,29,33	SOC_I2C0_SDA	<<	SOC_I2C0_SDA
	15,29,33	SOC_I2C0_SDA	<<	SOC_I2C0_SDA
From clock Buffer	31	PRG0_HSE_ETH1_CLK	<<	PRG0_HSE_ETH1_CLK
	31	PRG0_HSE_ETH2_CLK	<<	PRG0_HSE_ETH2_CLK
To and from ICSSG1 RGMII 2 Ethernet PHY	17	PRG1_RGMII2_R0	<<	PRG1_RGMII2_R0
	17	PRG1_RGMII2_RD1	<<	PRG1_RGMII2_RD1
	17	PRG1_RGMII2_RD2	<<	PRG1_RGMII2_RD2
	17	PRG1_RGMII2_RXC	<<	PRG1_RGMII2_RXC
	17	PRG1_RGMII2_RX_CTL	<<	PRG1_RGMII2_RX_CTL
	17	PRG1_ETH2_LED_1000RX_ER	<<	PRG1_ETH2_LED_1000RX_ER
	17	PRG1_RGMII2_T0	<<	PRG1_RGMII2_T0
	17	PRG1_RGMII2_TD1	<<	PRG1_RGMII2_TD1
	17	PRG1_RGMII2_TD2	<<	PRG1_RGMII2_TD2
	17	PRG1_RGMII2_TD3	<<	PRG1_RGMII2_TD3
	17	PRG1_RGMII2_TXC	<<	PRG1_RGMII2_TXC
	17	PRG1_RGMII2_TX_CTL	<<	PRG1_RGMII2_TX_CTL
	17,18	PRG1_MDIO_MDIO	<<	PRG1_MDIO_MDIO
	17,18	PRG1_MDIO_MDC	<<	PRG1_MDIO_MDC
	18	PRG1_ETH3_LED_LINK	<<	PRG1_ETH3_LED_LINK
	18	PRG1_ETH2_LED_LINK	<<	PRG1_ETH2_LED_LINK
To and from ICSSG2 RGMII 1 Ethernet PHY	18	PRG1_RGMII1_R0	<<	PRG1_RGMII1_R0
	18	PRG1_RGMII1_RD1	<<	PRG1_RGMII1_RD1
	18	PRG1_RGMII1_RD2	<<	PRG1_RGMII1_RD2
	18	PRG1_RGMII1_RD3	<<	PRG1_RGMII1_RD3
	18	PRG1_RGMII1_RXC	<<	PRG1_RGMII1_RXC
	18	PRG1_RGMII1_RX_CTL	<<	PRG1_RGMII1_RX_CTL
	18	PRG1_ETH3_LED_1000RX_ER	<<	PRG1_ETH3_LED_1000RX_ER
	18	PRG1_RGMII1_T0	<<	PRG1_RGMII1_T0
	18	PRG1_RGMII1_TD1	<<	PRG1_RGMII1_TD1
	18	PRG1_RGMII1_TD2	<<	PRG1_RGMII1_TD2
	18	PRG1_RGMII1_TD3	<<	PRG1_RGMII1_TD3
	18	PRG1_RGMII1_TXC	<<	PRG1_RGMII1_TXC
	18	PRG1_RGMII1_TX_CTL	<<	PRG1_RGMII1_TX_CTL
From MUX To HSE	16	HSE_PRG0_PRU1_GPO7	<&	

# GPMC



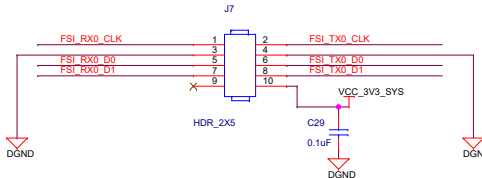
## GPMC TO FSI & HSE CONNECTOR



TS3A27518ERTWR Truth Table

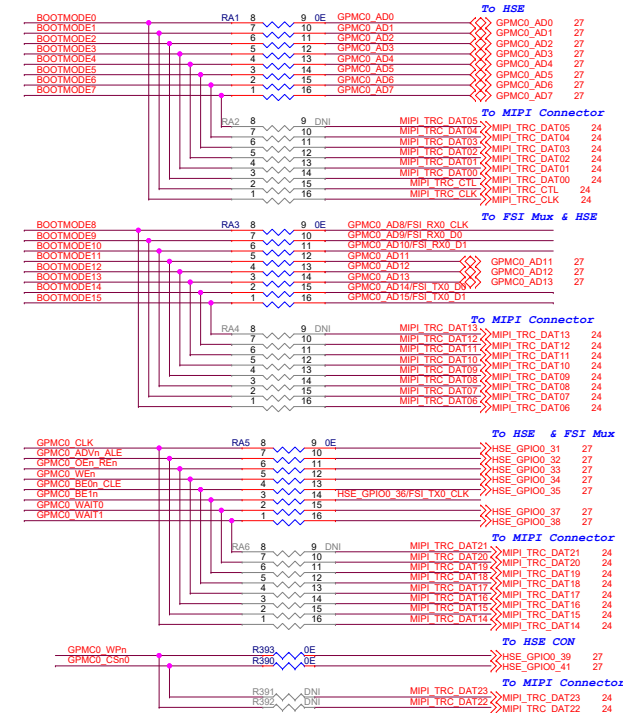
EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM1/2/3 & COM1/2/3 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & COM1/2/3 TO NO1/2/3	NC4/5/6 TO COM1/2/3 & COM1/2/3 TO NC4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

## FSI CONNECTOR



0- Ohm Res MUX between HSE Connector and TRACE Functionality

-For HSE Connector RA1, RA3, RA5, R393 & R390 Should be installed and RA2, RA4, RA6, R391& R392 Should be DNI'd.  
-For TRACE RA2, RA4, RA6, R391& R392 Should be installed and RA1, RA3, RA5, R393 & R390 Should be DNI'd.



## Off Page Connections

From IO Expander	33	FSI_FET_SEL	FSI_FET_SEL
To HSE Connector	27	GPMC0_CS#1	GPMC0_CS#1
	27	GPMC0_CS#2	GPMC0_CS#2
	27	GPMC0_CS#3	GPMC0_CS#3
	27	GPMC0_DIR	GPMC0_DIR
From FSI mux	27	GPMC0_AD8	GPMC0_AD8
To HSE Connector	27	GPMC0_AD9	GPMC0_AD9
	27	GPMC0_AD10	GPMC0_AD10
	27	GPMC0_AD14	GPMC0_AD14
	27	GPMC0_AD15	GPMC0_AD15
	27	HSE_GPIO0_36	HSE_GPIO0_36

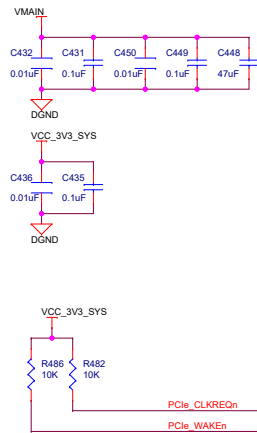
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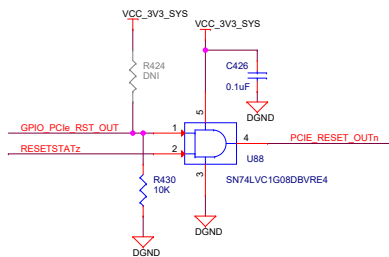
Title	GPMC
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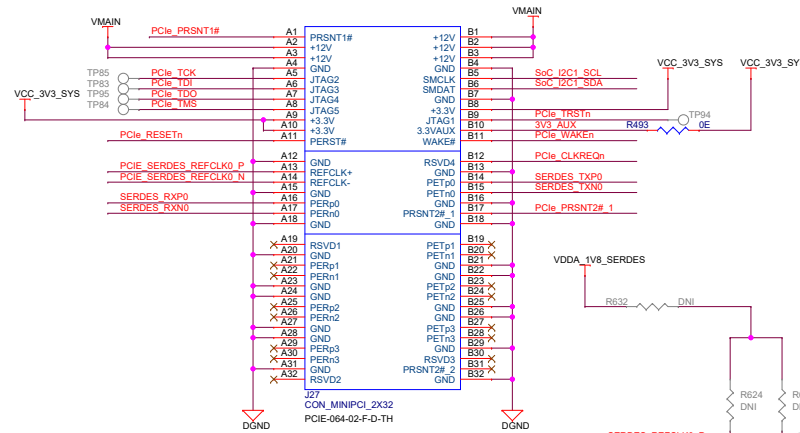
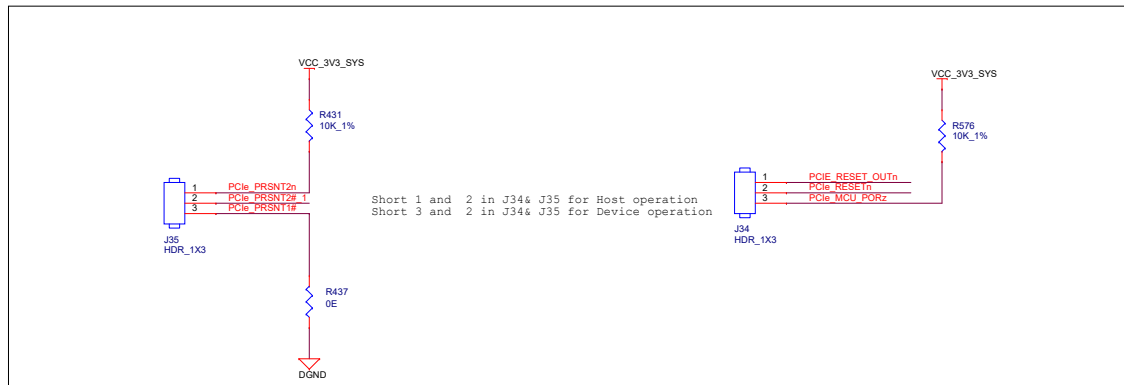
## x4 Lane PCIe Connector



### PCIe Reset

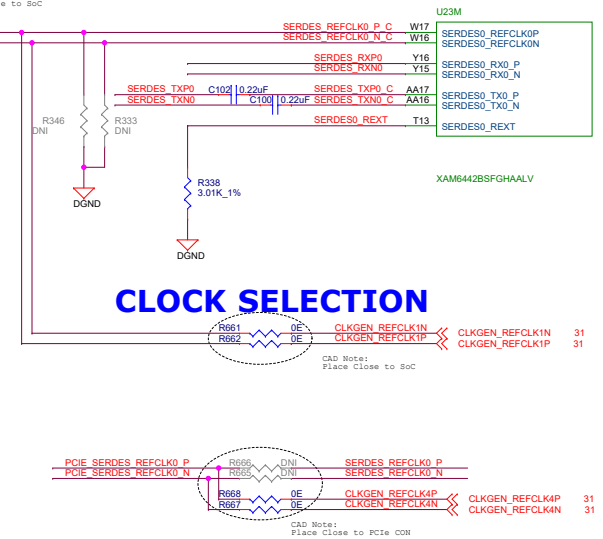


### RC OR EP MODE SELECTION



Note:  
R679 , R680 Mounted with 0E Resistor when PCIe REFCLK is in no Re-biasing Mode.  
R679 , R680 to be replaced with 100nf CAP 0402 package when PCIe REFCLK is in Re-biasing Mode.

### CLOCK SELECTION



### Off Page Connections

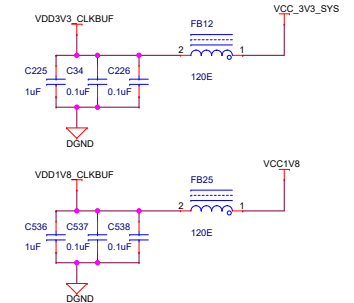
PCIE_MCU_PORz	PCIE_MCU_PORz	34
GPIO_Pcie_RST_OUT	GPIO_Pcie_RST_OUT	33
RESESTATz	RESESTATz	13,14,20,31,33,34
SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,31,32,33
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,31,32,33

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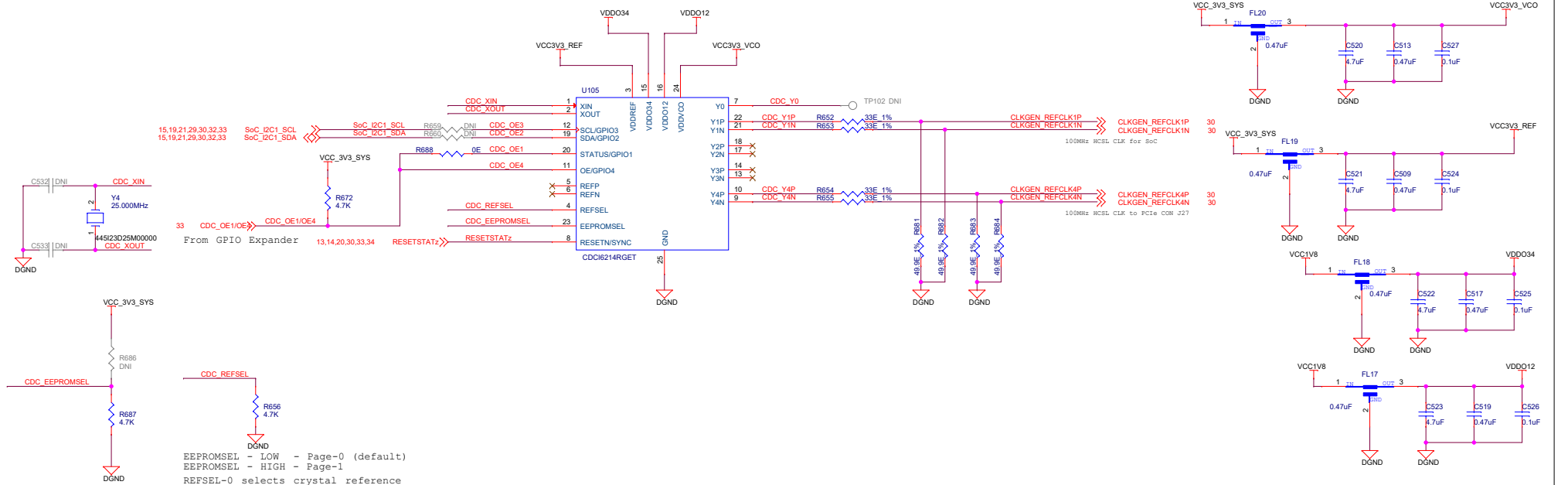


Title		
PCIe INTERFACE		
Size	PROC101C(004) TMD84EVM	Rev
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## ETHERNET PHY CLOCK BUFFER



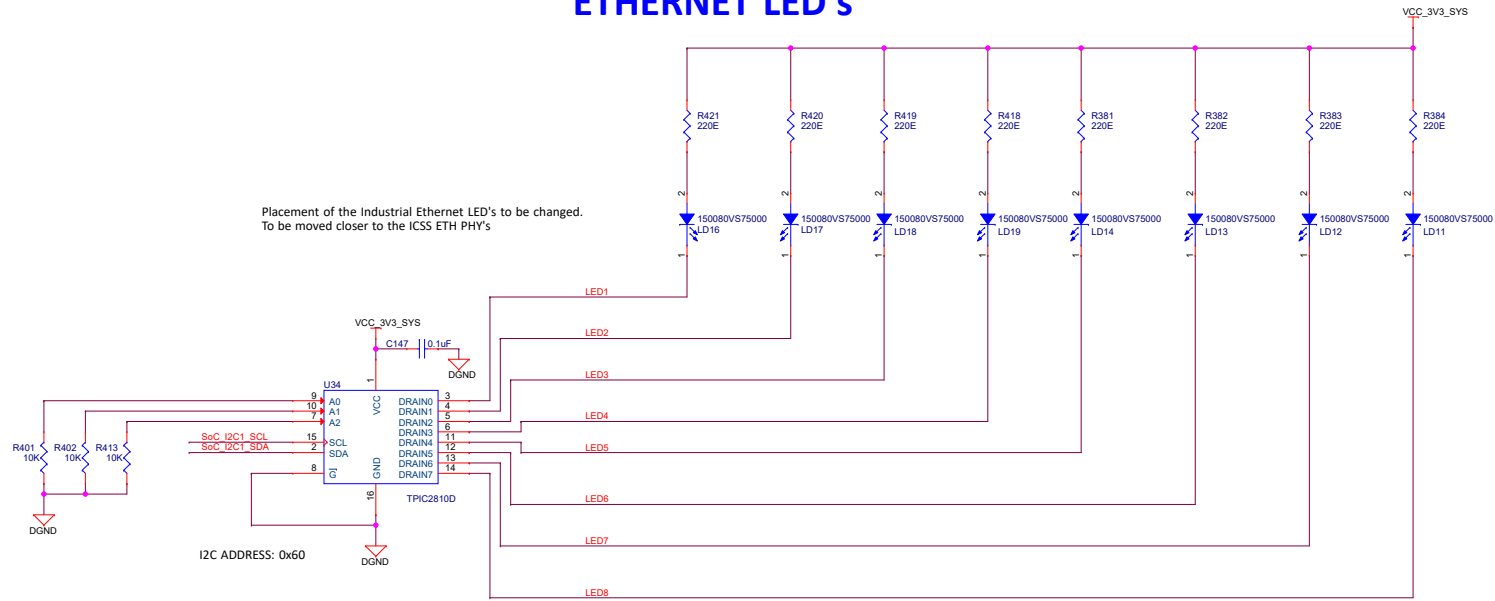
From SoC CLKOUT0  CLKOUT0 29



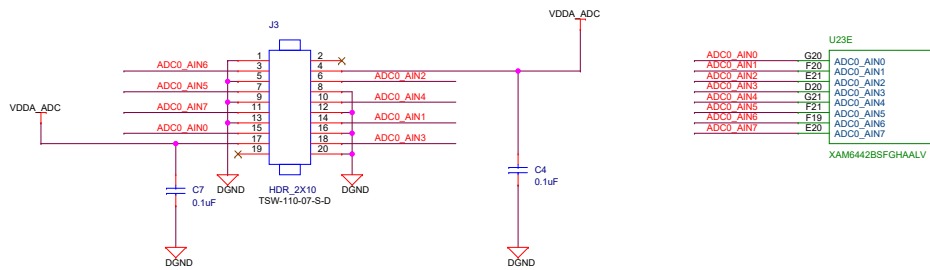
Size	Variant Name = PROC101C(004) TMD564EVM
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## ETHERNET LED's



## ADC CONNECTOR



### Off Page Connections

SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,30,31,33
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,30,31,33

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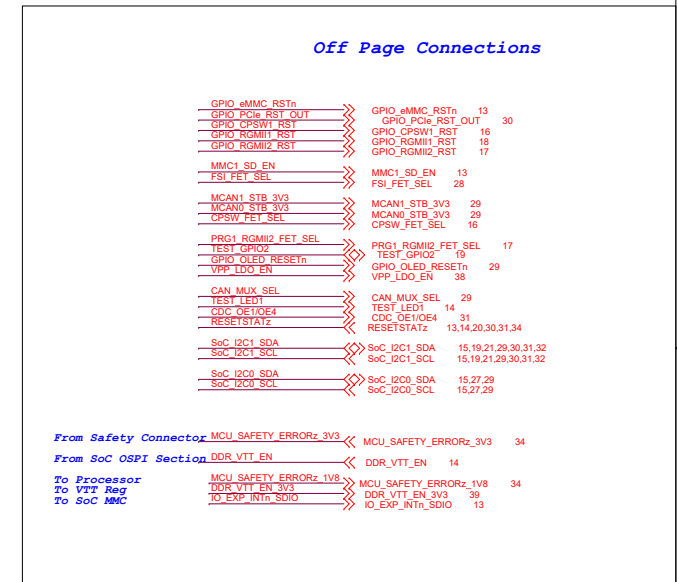
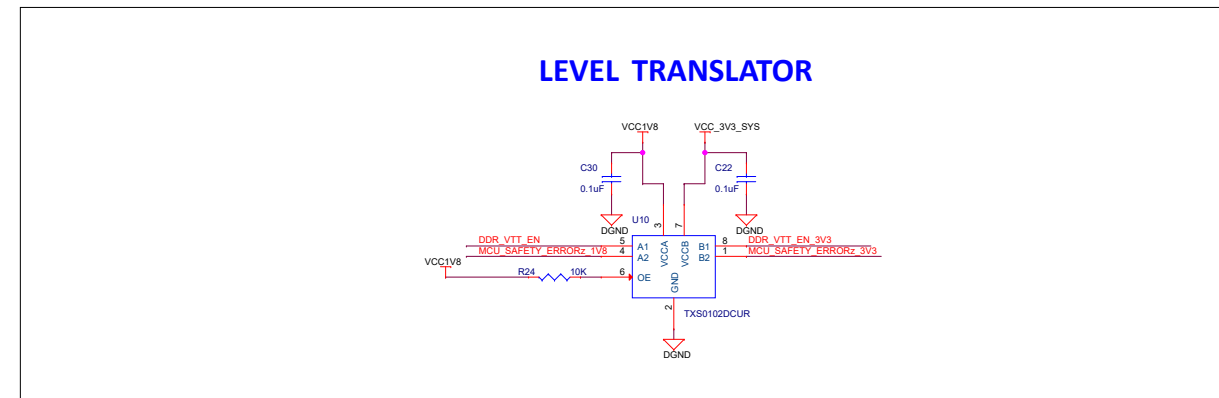
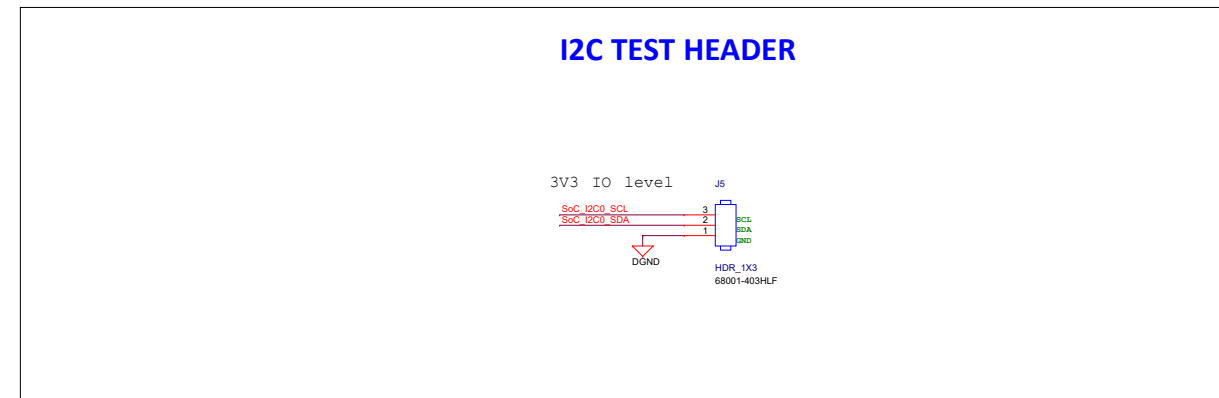
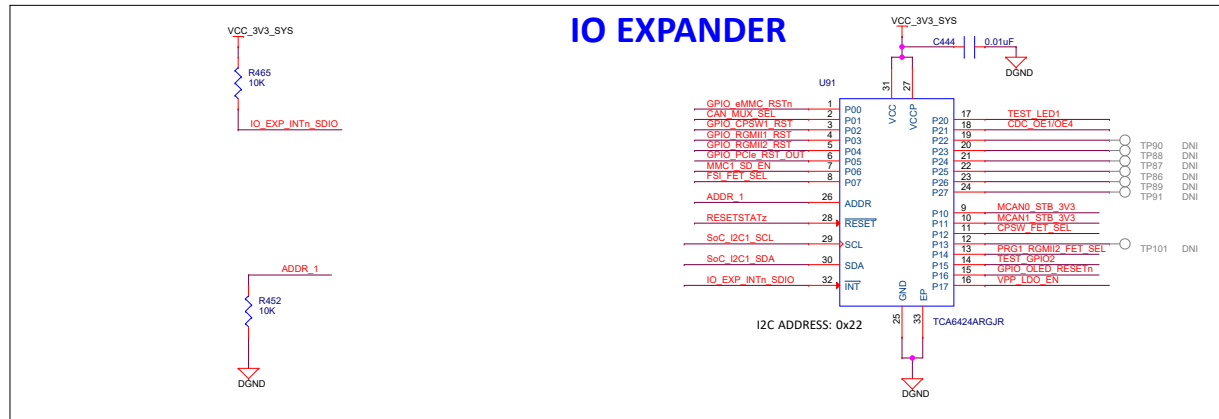


Title	ETHERNET LEDs
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Size	Variant Name = PROC101C(004) TMD564EVM
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The **MCU\_GENERAL** section includes the following components and connections:

- U23H (MCU)**:
  - Power**: VCC\_3V3\_SYS connected to pins A10, A11, B10, B11, C21, and B20.
  - GPIOs**:
    - GPIO0\_7 (D7) to GPIO0\_6 (B7) connected to DGN.
    - GPIO0\_9 (C9) to GPIO0\_8 (C8) connected to DGN.
    - GPIO0\_9 (C9) to TEST\_LED2 (A7) connected to DGN.
    - GPIO0\_6 (B7) to UART0\_RX\_3V3 (A9) and UART0\_TX\_3V3 (A8) connected to DGN.
    - GPIO0\_9 (C9) to UART1\_RX\_3V3 (C9) and UART1\_TX\_3V3 (D9) connected to DGN.
    - GPIO0\_9 (C9) to UART0\_CTS\_3V3 (D8) and UART0\_RTS\_3V3 (E8) connected to DGN.
    - GPIO0\_9 (C9) to UART1\_CTS\_3V3 (B8) and UART1\_RTS\_3V3 (B9) connected to DGN.
  - UARTs**:
    - UART0\_RX\_3V3 (A9) and UART0\_TX\_3V3 (A8) connected to DGN.
    - UART1\_RX\_3V3 (C9) and UART1\_TX\_3V3 (D9) connected to DGN.
    - UART0\_CTS\_3V3 (D8) and UART0\_RTS\_3V3 (E8) connected to DGN.
    - UART1\_CTS\_3V3 (B8) and UART1\_RTS\_3V3 (B9) connected to DGN.
  - Other**:
    - MCU\_I2C0\_SCL (E9) and MCU\_I2C0\_SDA (A10) connected to DGN.
    - MCU\_I2C1\_SCL (A11) and MCU\_I2C1\_SDA (B10) connected to DGN.
    - MCU\_OSC0\_XI (C21) and MCU\_OSC0\_XO (B20) connected to DGN.
    - MCU\_SPI0\_CLK (E7) and MCU\_SPI0\_D0 (B6) connected to DGN.
    - MCU\_SPI0\_D1 (B6) and MCU\_SPI0\_CS0 (D6) connected to DGN.
    - MCU\_SPI0\_CS1 (C6) and MCU\_SPI0\_CS1 (C6) connected to DGN.
- U23C (MCU)**:
  - Power**: VCC\_3V3\_SYS connected to pins A20, B21, E17, B12, B13, E18, and F16.
  - GPIOs**:
    - MCU\_SAFETY\_ERRORz\_1V8 (A20) connected to DGN.
    - MCU\_PORz (B21) connected to DGN.
    - PORz\_OUT (E17) connected to DGN.
    - MCU\_RESETz (B12) connected to DGN.
    - MCU\_RESETSTATz (B13) connected to DGN.
    - SoC\_WARM\_RESETz (E18) connected to DGN.
    - RESETSTATz (F16) connected to DGN.
  - Other**:
    - EXTINTN (A20) connected to DGN.
    - MCU\_RESETz (B12) connected to DGN.
    - MCU\_RESETSTATz (B13) connected to DGN.
    - RESET\_REQz (E18) connected to DGN.
    - RESETSTATz (F16) connected to DGN.
- SN74LVC1G11DCKR (Comparator)**:
  - Power**: VCC1V8 connected to pins 1, 3, 4, and 6.
  - Inputs**:
    - Pin 1: PORz (35).
    - Pin 3: CONN MCU PORz (30).
    - Pin 4: MCU PORz (30).
    - Pin 6: PCIE MCU PORz (30).
  - Output**:
    - Pin 2: SN74LVC1G11DCKR output connected to DGN.

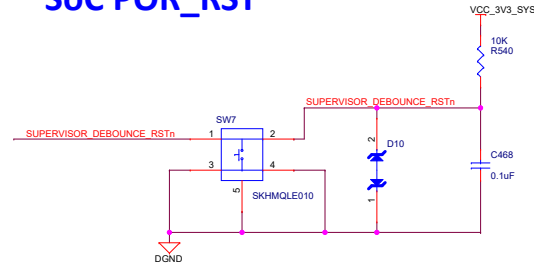
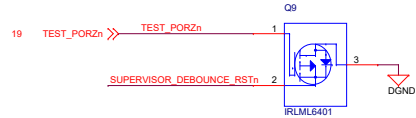
Figure 1: Schematic diagram of the processor power-up sequence. The diagram shows the internal components of the processor, including the oscillator (Y1, 25.000MHz), capacitors (C133, C134, C138, C139), resistors (R137, R138, R139, R140), and the MCU oscillator pins (MCU\_OSC0\_XI, MCU\_OSC0\_XO). It also shows the power supply pins (VCC\_3V3\_SYS, VCC\_3V3\_SYS, VCC\_3V3\_SYS) and the reset pin (MCU\_RESETz). The diagram is labeled 'Figure 1: Schematic diagram of the processor power-up sequence'.

To HSE Connector	MCU_RESETSTATz	MCU_RESETz	27,35	
		MCU_RESETSTATz	27	
To level translator	MCU_SAFETY_ERRORz_3V3	MCU_SAFETY_ERRORz_3V3		33
To level translator	MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8		33
To Boot Mode Section	PORz_OUT	PORz_OUT	13,16,17,18,20	
From ICSSG Phyl62	PRG1_RGMII_InTn	PRG1_RGMII_InTn	16,17,18	
To User LED	TEST_LED2	TEST_LED2	14	
From Push button	MCU_GPIO0_6	MCU_GPIO0_6	35	
Switch				
	SoC_CLKIN	SoC_CLKIN	31	
	MCU_UART0_RX_3V3	MCU_UART0_TX_3V3	26	
	MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	26	
	MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	26	
	MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	26	

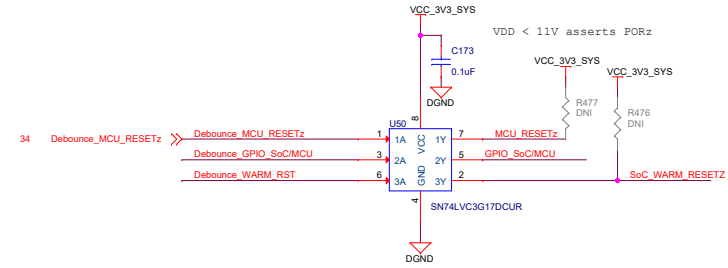


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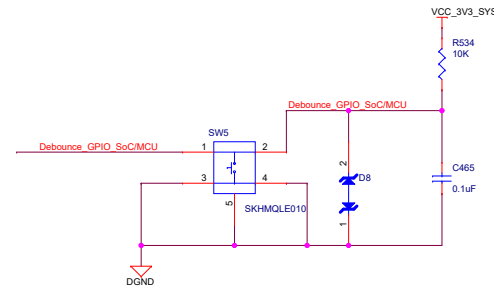
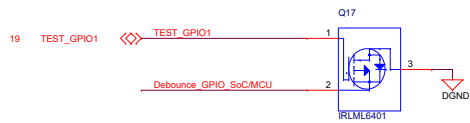
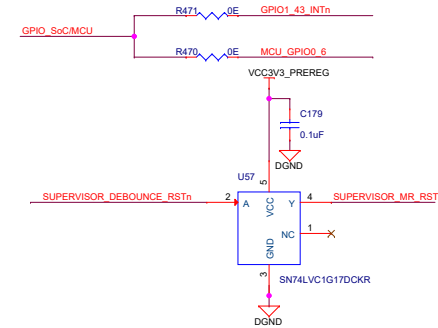
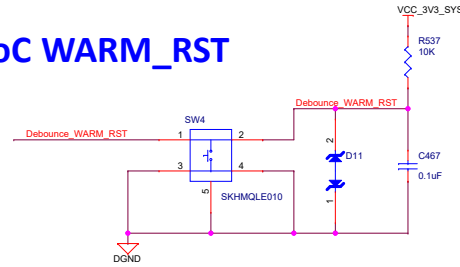
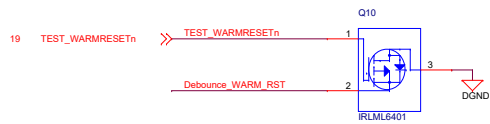
## SoC POR\_RST



## DEBOUNCE CIRCUIT



## SoC WARM\_RST

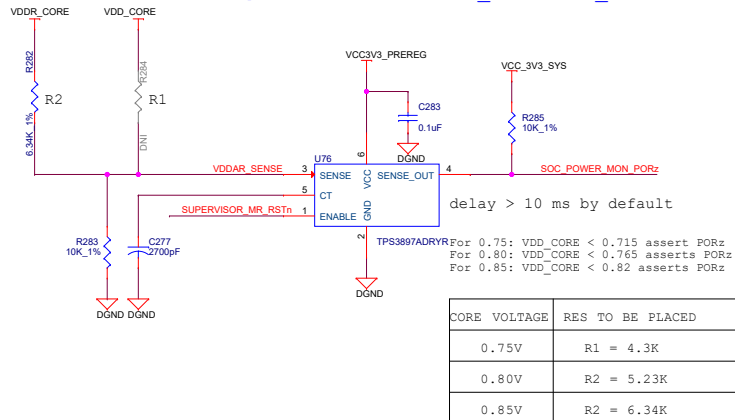


## Off Page Connections

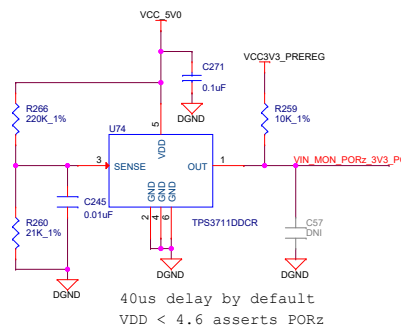
To Processor	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG	37,39
	SoC_WARM_RESETz	SoC_WARM_RESETz	34
	GPIO1_43_INTn	GPIO1_43_INTn	29
	MCU_RESETz	MCU_RESETz	27,34
	MCU_GPIO0_6	MCU_GPIO0_6	34

## VOLTAGE SUPERVISOR

### Core Voltage Monitor (VDDAR\_CORE/VDD\_CORE)



### 5V OUTPUT MONITOR (VCC\_5V0)



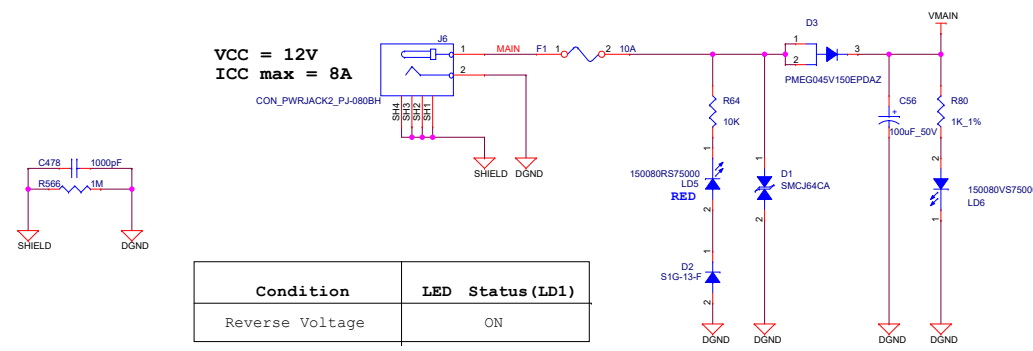
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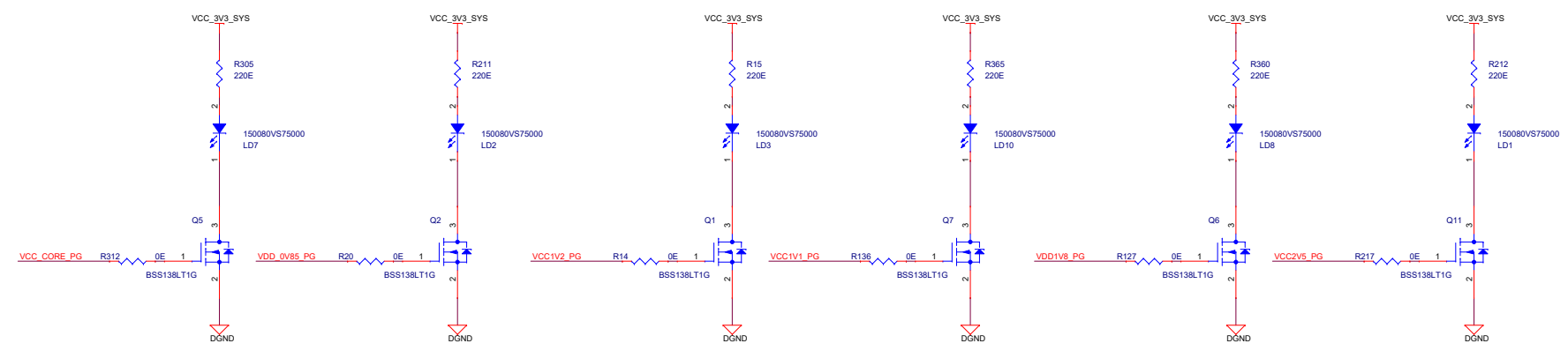
Title DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR

Size	Variant Name = PROC101C(004) TMD564EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 35 of 40

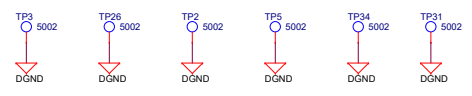
MAIN INPUT 12V DC



POWER INDICATION LED'S



Ground test points



Off Page Connections

VCC_CORE_PG	VCC_CORE_PG	37,38
VDD_0V85_PG	VDD_0V85_PG	38
VCC1V2_PG	VCC1V2_PG	38
VCC1V1_PG	VCC1V1_PG	38
VDD1V8_PG	VDD1V8_PG	39
VCC2V5_PG	VCC2V5_PG	38

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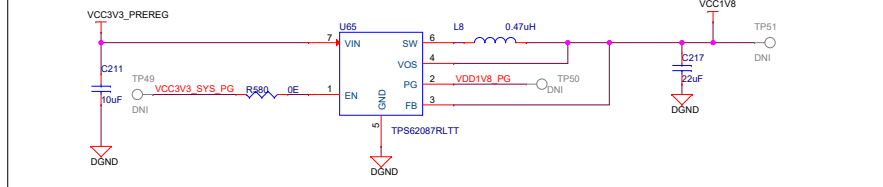


Title MAIN 12V POWERSUPPLY		
Size	Variant Name = PROC101C(004) TMD564EVM	
C	E2	
Date:	Thursday, August 18, 2022	Sheet 36 of 40

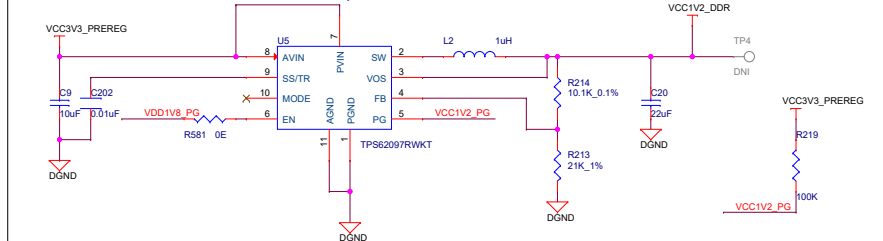


## SoC POWER SUPPLY

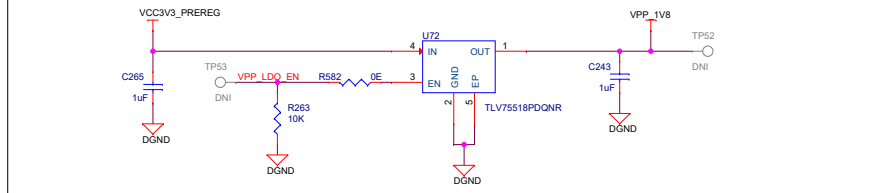
### 1.8V IO, 3.0AMPS SUPPLY



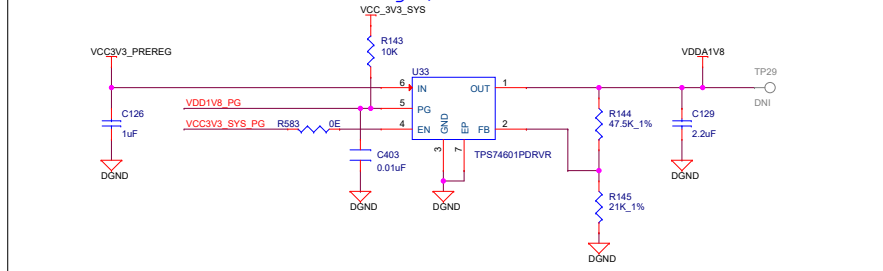
### 1.2V, 2.0AMPS SUPPLY



### 1.8V VPP, 0.15AMPS SUPPLY



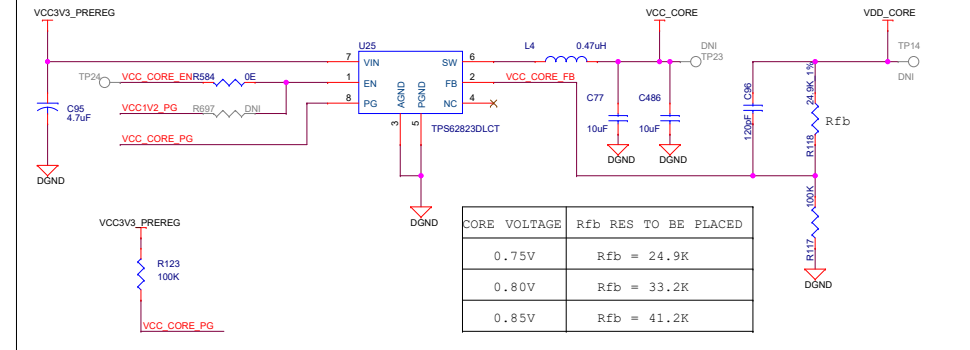
### 1.8V Analog , 1AMPS SUPPLY



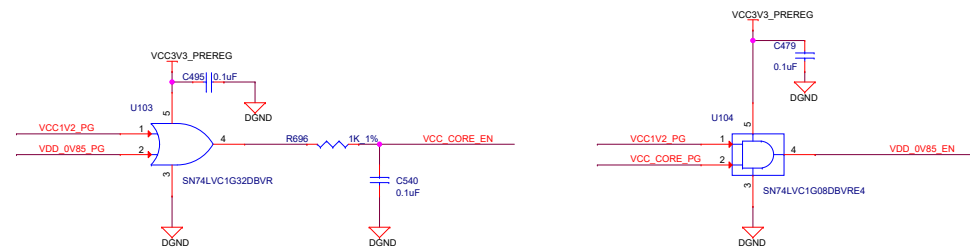
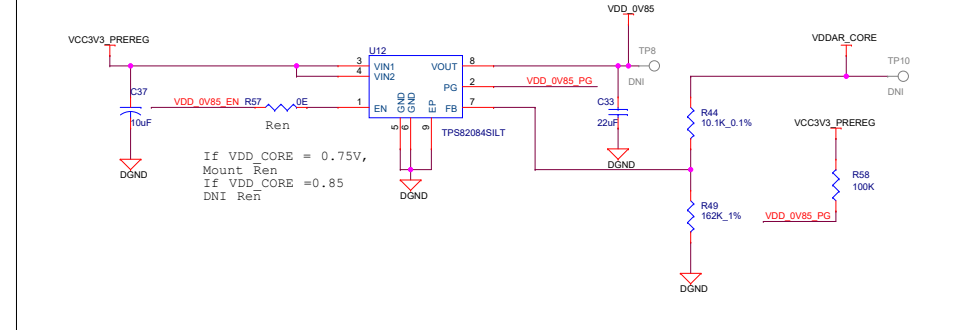
#### Off Page Connections

36.37	VCC_CORE_PG	VCC_CORE_PG
36	VDD_OV85_PG	VDD_OV85_PG
36	VCC1V2_PG	VCC1V2_PG
36	VDD1V8_PG	VDD1V8_PG
36	VPP_LDO_EN	VPP_LDO_EN
33	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG
35,37,39	VCC3V3_SYS_PG	VCC3V3_SYS_PG

### 0.75 / 0.8 / 0.85V, 3.0AMPS SUPPLY



### 0.85 V, 1.5AMPS SUPPLY



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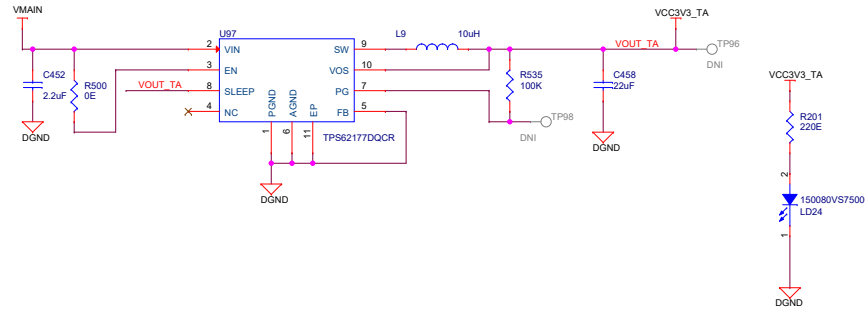


Title SoC POWER SUPPLY

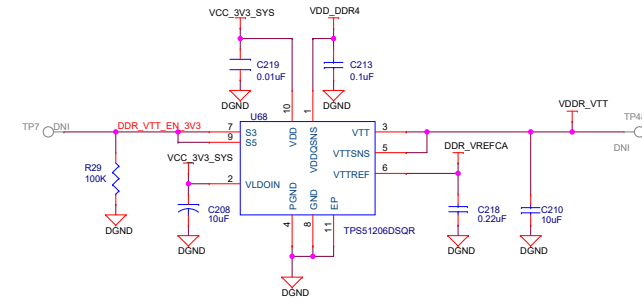
Size	Variant Name = PROC101C(004) TMD564EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 38 of 40

# PERIPHERAL POWER SUPPLY

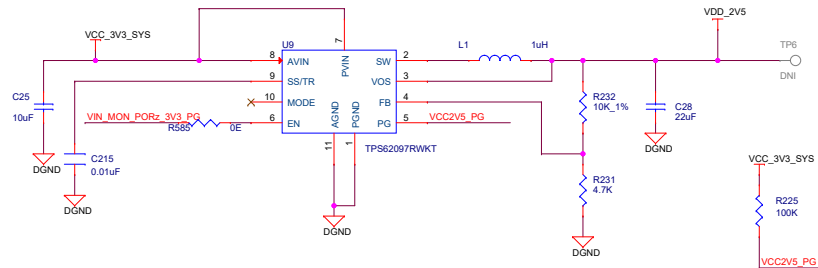
## TEST AUTOMATION BOARD POWER



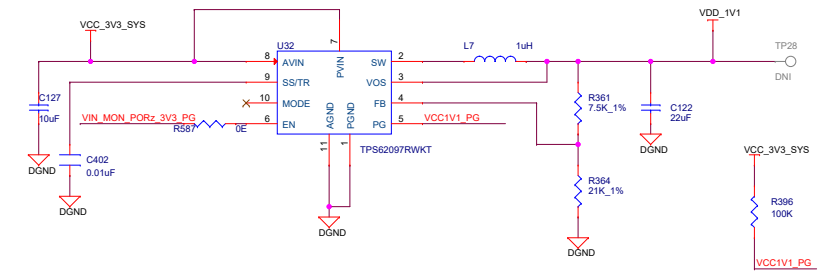
## VTT SUPPLY FOR DDR4



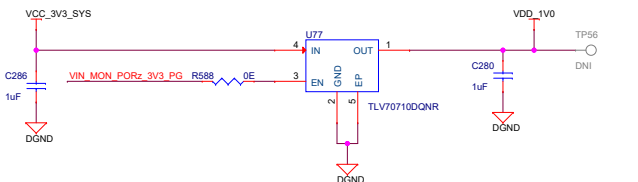
## 2.5V, 2.0AMPS SUPPLY



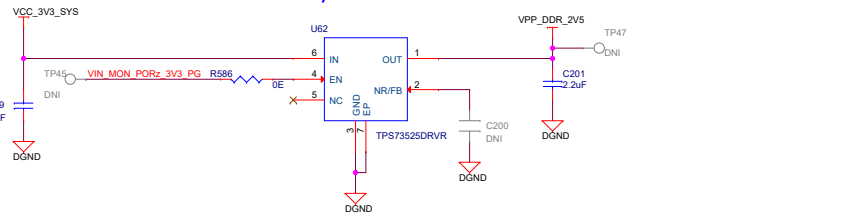
## 1.1V ETHERNET PHY POWER SUPPLY



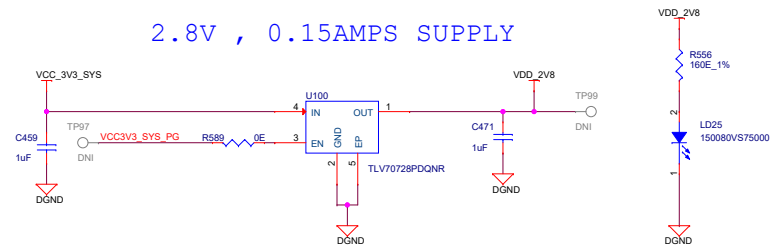
## 1.0V ETHERNET PHY POWER SUPPLY



## 2.5V, .5 AMPS SUPPLY



## 2.8V , 0.15AMPS SUPPLY



### Off Page Connections

33	DDR_VTT_EN_3V3	DDR_VTT_EN_3V3
36	VCC2V5_PG	VCC2V5_PG
36	VCC1V1_PG	VCC1V1_PG
37,38	VCC3V3_SYS_PG	VCC3V3_SYS_PG
35,37	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG

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Title PERIPHERAL POWER SUPPLY

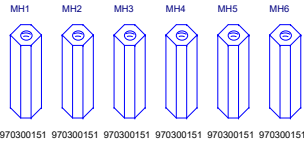
Size	Variant Name = PROC101C(004) TMD564EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 39 of 40

HARDWARE SCHEMATICS

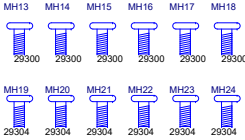
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

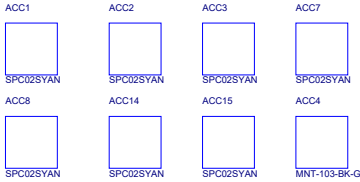
STANDOFFS



SCREWS



JUMPERS



WASHER'S



FIDUCIALS



RUBBER FEET



TI EVM FLYERS



Socket & Processor as Accessories



BARE PCB



LABELS

Board Serial No.



Assembly Revision

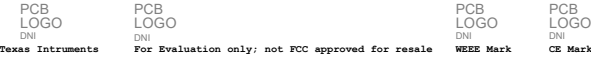


ORDERABLE PART NO



Orderable part number	
Variant	Label Text
001	TMDS64GPEVM
002	TMDS243GPEVM
003	TMDS64HSEVM
004	TMDS64EVM
005	TMDS243EVM

LOGOs



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Title HARDWARE SCHEMATICS

Size	Variant Name = PROC101C(004) TMD564EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 40 of 40